Fast Transient Analysis of Power Distribution Network Modeled by Unstructured Meshes by Using Locally Implicit Latency Insertion Method

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***Abstract*—This paper proposes a locally implicit latency insertion method (LILIM), which is a suitable method for the fast simulation of an arbitrary shaped power distribution network (PDN) modeled by triangular meshes. First, an efficient modeling method based on triangular mesh is reviewed and we refer to the limitation of the LIM for the meshed PDN analysis. Next, in order to overcome the problem, we formulate the LILIM by combining the efficient modeling and the locally implicit schemes. Finally, the numerical results show that the LILIM is applicable and efficient for the simulation of the PDN analysis.**

***Index Terms*—Delaunay triangular mesh, latency insertion method, locally implicit finite difference method, power distribution network, time-domain analysis, Voronoi tessellation.**

I. Introduction

Recent semiconductor packaging technologies have enabled integrated circuits (ICs) to be assembled within an extremely small area. To provide power to each system, an irregular shaped power distribution networks are arranged in chips, packages, and boards. However, the simultaneous switching noise (SSN) induced by increased power density and shorter signal edges directly degrades the power/signal integrity (PI/SI) of the recent low-voltage PDN. In order to guarantee PI/SI of the system composed of the chips, packages, and boards, the PDN must be modeled and simulated efficiently and accurately. One of the useful approaches for modeling and simulation is the finite different method using square meshes [1]. This method can simulate efficiently the PDN with apertures. However, modeling of the PDN using square meshes suffers from the staircase approximation error when the PDN contains small features such as via holes, small apertures, plane gaps and so on. Another approch for the PDN modeling is one using triangular meshes instead of the square ones [2], [3]. This type of modeling method usually uses the Delaunary triangulation, which genarates the Delaunay mesh and Voronoi tessellation, which are mutually orthogonal to each other. This property of the mesh geometry is important in the sense that electric and magnetic fields are orthogonal to each other. These modeling methods achieve successfully to reduce the total number of unknown variables without degrading the accuracy for the modeling of the fine geometric structure compared with that of the square meshes.

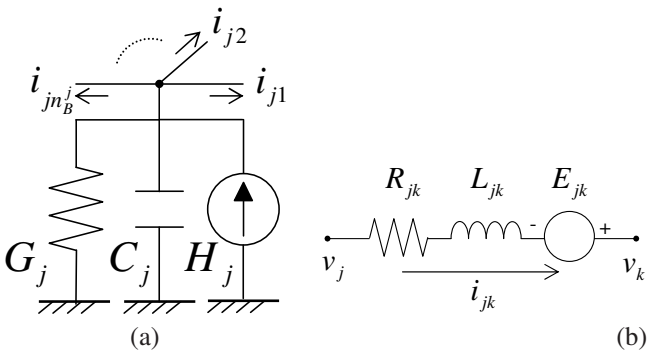

Fig. 1. Network topologies required for LIM. The arrows correspond to directions of the branch currents. (a) Node topology. (b) Branch topology.

On the other hand, the latency insertion method (LIM) has been proposed as one of the fast circuit simulation techniques [4]. The LIM is suitable to simulate an equivalent circuit extracted by the modeling methods with triangular meshes since the equivalent circuit satisfies the required topologies, where each node and branch contain the grounded capacitance C and the serial inductance L as shown in Fig. 1, respectively. However, the LIM has the constraint of time step size to satisfy the numerical stability condition similar to the FDTD method since the method is based on the explicit leapfrog scheme [4], [5], [6]. Concretely, the maximum time step size is limited by the minimum values of C and L in the computational domain. The values of C and L in the equivalent circuit are proportional to the size of each triangular mesh. Thus, the maximum time step size of the LIM is extremely dependent on these values

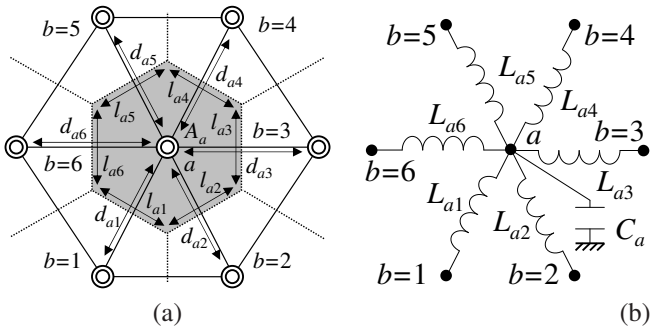

Fig. 2. Voronoi diagram and triangular mesh for conductor media. (a) Double circle, dash lines, and solid lines indicate the Voronoi point, the Voronoi region, and triangular mesh. (b) Equivalent circuit, where grounded resistance G and series resistance R are not shown, of triangular mesh, where vertices and edges of triangular mesh are corresponding to nodes and branches.

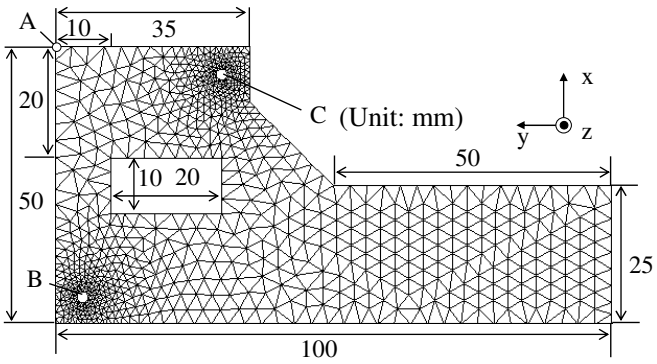

Fig. 3. Top view of an example PDN modeled by triangular meshes.

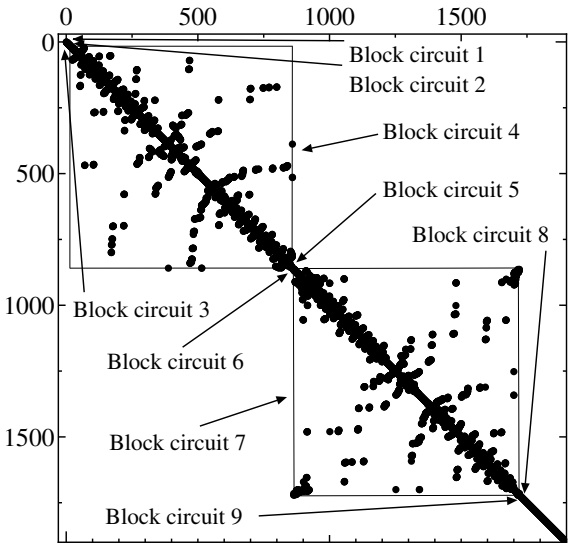

Fig. 4. Coefficient matrix structure of $\{v\}$ in the LILIM.

since the vicinities of fine structures are modeled by exploiting the tiny size of triangular meshes. As a consequence, a large amount of computational cost is required even if the LIM, which is much faster than matrix-based SPICE-like simulators, is employed.

In this paper, we propose the locally implicit (LI) LIM to overcome the inherent problem of the LIM. The LILIM employs a locally implicit scheme instead of the globally explicit leapfrog scheme used in the original LIM The similar approaches have been applied to the FDTD method [7], [8]. These approaches apply the implicit scheme to one direction in which the space is discretized into smaller cells than those in the other directions. By contrast, in our proposed LILIM, the implicit scheme is applied to the local area which is composed of small values of reactance elements.

The remainder part of the paper is organized as follows. In Section II, the modeling method by using the triangular meshes is reviewed. Section III describes the formulations and features of the proposed LILIM. Section IV demonstrates accuracy and efficiency of the proposed method by showing some numerical examples, and conclusions are given in Section V.

II. PDN Modeling by Using Triangular Meshes

In modeling of the arbitrary shaped PDN, square meshes must be globally tiny even if the fine structure is contained in the local region. This fact leads that the number of unknown variables increases drastically. Additionally, the square mesh scheme suffers from the staircase approximation on the edge of the geometric structure. In order to cope with the above inherent problems, the efficient modeling methods based on triangular meshes have been proposed [2], [3]. These methods successfully reduce the total number of unknowns without degrading the accuracy since the triangular mesh scheme is flexible to capture the complex structures by resizing the mesh sizes locally. These triangular meshes are lead by Delaunay Triangularization and Voronoi Tessellation as shown in Fig. 2(a). In Fig. 2(a), the gray hexagonal part indicates the area A_a of Voronoi region surrounding Voronoi point a, and d_{ab} and I_{ab} indicate the length of the Voronoi edge and the length of the edge in triangular mesh, respectively. The equivalent circuit is extracted from the object meshed triangularly, as shown in Fig. 2(b), where the Voronoi point and the side of triangular mesh correspond to the node and branch topologies. And the circuit is composed of the grounded capacitances and inductances of which the values are derived by the following manner:

$$C_a = \varepsilon \frac{A_a}{h}, \quad L_{ab} = \mu h \frac{d_{ab}}{l_{ab}}, \tag{1}$$

where ε, μ, and h indicate permittivity, permeability, and dielectric thickness. It is confirmed that the equivalent circuit extracted from the triangular meshes has the topologies, in which every node and branch contains the grounded capacitance C and the serial inductance L. Therefore, the equivalent circuit is suitable to be solved by using the basic LIM. For example (1) means that the value of C_a is proportional to A_a, and the arbitrary shaped PDN model is constructed by the various values of capacitance according to the mesh sizes. Thus, the maximum time step size of the basic LIM is strictly

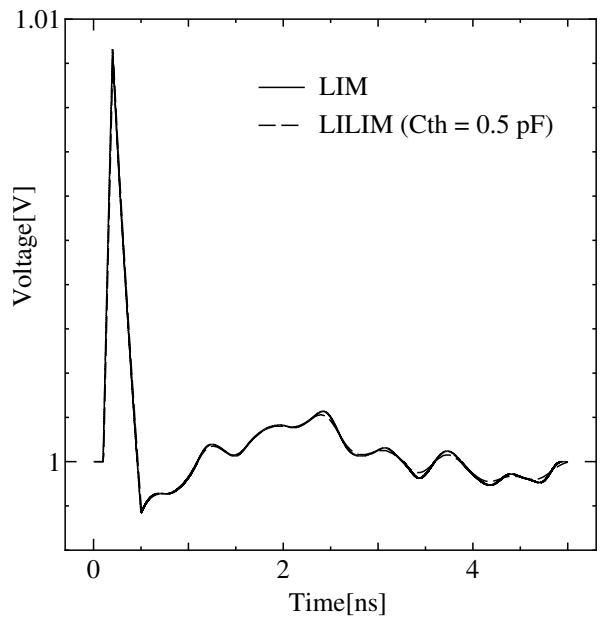

Fig. 5. Waveform results at the port C.

limited by the reactance element values as mentioned in [5].

III. LILIM FOR THE MESHED PDN

In order to simulate efficiently the arbitrary shaped PDN modeled by triangular meshes, we propose and formulate the LILIM by employing locally implicit scheme instead of globally explicit leapfrog scheme. First, the Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) are applied to the node a and the branch ab in Fig. 2, and the differential equations are given by

$$C_a \frac{dv_a}{dt} + G_a v_a = -\sum_{b=1}^{N_B^a} i_{ab}, \tag{2}$$

$$L_{ab} \frac{di_{ab}}{dt} + R_{ab} i_{ab} = v_a - v_b, \tag{3}$$

where v_a, i_{ab}, and N_B^a indicate the voltage at the node a, the current flowing from the node a to the node b, and the total number of branches connecting to the node a. Next, the term of the branch currents connecting to the node a in (2) is split into two terms, which are accompanied with the capacitance larger than the threshold capacitance C_{th} and less than C_{th}. In this paper, the former can be regarded as branch topology, on the other hand, the latter is defined as *branch block*. Next, by applying the leapfrog scheme [4], [5] and the implicit scheme to the branch topology and the branch block respectively in (2), then, the following equation is derived;

$$v_a^{n+\frac{1}{2}} = \frac{C_a}{\alpha_a} v_a^{n-\frac{1}{2}} + \frac{\Delta t}{\alpha_a} \left(- \sum_{m=1}^{N_L} i_{am}^n - \sum_{m=1}^{N_S} i_{am}^{n+\frac{1}{2}} \right), \tag{4}$$

where $\alpha_a = (C_a + \Delta t G_a)$, $N_L + N_S = N_B^a$, and N_L and N_S are the total numbers of the branch topologies and branch blocks. n denotes the time index, and Δt is the time step size. In (4), the node voltage and the branch currents in branch block are arranged at the same time step. Thus, to update the unknown variables, simultaneous equations must be solved. $i_{am}^{n+\frac{1}{2}}$ given by the implicit difference of (3), namely (5),

$$i_{am}^{n+\frac{1}{2}} = \frac{L_{am}}{\beta_{am}} i_{am}^{n-\frac{1}{2}} + \frac{\Delta t}{\beta_{am}} \left(v_a^{n+\frac{1}{2}} - v_m^{n+\frac{1}{2}} \right), \tag{5}$$

is substituted into the terms of branch blocks in (4), where $\beta_{am} = (L_{am} + \Delta t R_{am})$. Then, (4) is transformed to

$$\left(1 + \frac{\Delta t}{\alpha_a} \sum_{m=1}^{N_S} \frac{\Delta t}{\beta_{am}} \right) v_a^{n+\frac{1}{2}} - \frac{\Delta t}{\alpha_a} \sum_{m=1}^{N_S} \left(\frac{\Delta t}{\beta_{am}} v_m^{n+\frac{1}{2}} \right)$$
$$= \frac{C_a}{\alpha_a} v_a^{n-\frac{1}{2}} + \frac{\Delta t}{\alpha_a} \left[- \sum_{m=1}^{N_L} i_{am}^n - \sum_{m=1}^{N_S} \left(\frac{L_{am}}{\beta_{am}} i_{am}^{n-\frac{1}{2}} \right) \right]. \tag{6}$$

In the left hand side of (6), there are plural unknown node voltages at the $(n + \frac{1}{2})$-th step. The node accompanied with the voltage variable $v_m^{n+\frac{1}{2}}$ is connected to the node a through the branch block.

This is caused by applying the implicit scheme to the currents in the branch blocks. Thus, in our proposed LILIM, we define the circuit in which the nodes are coupled with each other as a *block circuit*. By deriving the node-based equations in a block circuit, then, the updating formula of the block circuit is given by

$$(([I] + \Delta t[K_1]) + [K_2][M]) \{v\}^{n+\frac{1}{2}} = [K_3]\{v\}^{n-\frac{1}{2}} + \{b\}, \tag{7}$$

where $\{v\}$, $\{b\}$, $[K_{j=1,2,3}]$, $[M]$, and $[I]$ indicate the unknown voltage vector in the block circuit, the known vector, the coefficient matrices, the incidence matrix, and the unit matrix, respectively. The dimensions of the vectors and the matrices in (7) are defined as

$$\{v\}, \{b\} \in \Re^{N_{block}}, \quad [K_j], [M], [I] \in \Re^{N_{block} \times N_{block}},$$

where N_{block} denotes the number of the nodes in one block circuit. Equation (7) is solved by using a direct matrix solver, e.g. LU decomposition method. The computational cost is relatively smaller than the cost of the SPICE-like algorithm although the calculation cost increases as the size of the block

TABLE I
CPU TIME

Method	CPU Time [s]	Speed-up
LIM	59.719	1.00
LILIM	16.406	3.64

TABLE II
MEMORY UTILIZATION

Method	Memory utilization[M byte]
LIM	43
LILIM	145

circuit becomes larger, because the direct method is used only for the local block circuits similarly to the block-LIM [9].

In the proposed LILIM, the voltage variables in each block circuit are updated by (7). After that, the current variables in the branch block are updated explicitly by using (5). On the other hand, the unknown variables in the domain except for the block circuits are updated explicitly based on the following basic LIM updating formulas

$$v_a^{n+\frac{1}{2}} = \frac{C_a}{C_a + \Delta t G_a} v_a^{n-\frac{1}{2}} - \frac{\Delta t}{C_a + \Delta t G_a} \sum_{b=1}^{N_B^a} i_{ab}^n, \tag{8}$$

$$i_{ab}^{n+1} = \frac{L_{ab} - \Delta t R_{ab}}{L_{ab}} i_{ab}^n + \frac{\Delta t}{L_{ab}} (v_a^{n+\frac{1}{2}} - v_b^{n+\frac{1}{2}}). \tag{9}$$

The LILIM has the advantage similar to that of the HIE-FDTD method [7], [8], [10], which is locally free from the CFL condition. The maximum time step size of the LILIM does not depend on the value of the reactance elements in the block circuit. Thus, the LILIM can perform the efficient circuit simulation of the the arbitrary shaped network with various latencies.

IV. Numerical Results

In order to estimate the efficiency of the LILIM, an example PDN has been simulated by the basic LIM and LILIM. The shape and dimension of the PDN are shown in Fig. 3. The height of the dielectrics between the conductor planes is h = 0.6 mm, and its relative permittivity ε_r is 4.2. The conductor plane is discretized using the triangular meshes with 1890 nodes. The value of C_{th} is derived empirically and equals to 0.05 pF. In this case, 1890 nodes are classified into 165 node topologies and 9 block circuits, of which the numbers of the internal nodes are 1, 3, 16, 840, 1, 1, 860, 2, and 1, respectively. Fig. 4 shows the coefficient matrix of the unknown voltages generated by (7) and (8). In Fig. 4, each coefficient matrix of the block circuit is factored using the LU decomposition before the transient analysis. The maximum time step sizes used in the LIM and LILIM are 0.0267 ps and 3.15 ps, respectively. These values are evaluated by assuming the minimum value of capacitance and the value of C_{th} are less than the upper bound mentioned in [5]. The constant voltage source (= 1.0 V) is connected to the port A in Fig. 3. In addition, the input current source is connected to the port B in Fig. 3, and is the triangle wave of which the pulse value is 0.005 A, delay time is 0.1 ns, rise and fall times are 0.1 ns and 0.3 ns, and period is 0.5 ns. The simulation interval is [0 ns, 5 ns], and we observed the voltage waveform at the port C in Fig. 3.

The waveform results are illustrated in Fig. 5. It is confirmed that the waveform obtained from the LIM and LILIM agree well with each other. CPU times and memmory utilization of the LIM and LILIM are shown in Table I and II, respectively. From Table I, we can seee that the LILIM is about 3.64 times faster than the LIM. As a result, the proposed method is more effective than the conventional methods for the arbitrary shaped PDN analysis with appropriate accracy.

V. Conclusion

In this paper, an efficient LIM-based algorithm for the meshed PDN analysis based on locally implicit scheme has been proposed. The the time step size limitation in the LIM was alleviated by exploiting the advantages of the locally implicit-based algorithm. As a consequence, it has been verified that the LILIM can perform the fast circuit simulations using the larger time step sizes which are prohibited in the basic LIM analysis. The numerical results showed that the LILIM was about 3.64 times faster than the basic LIM without loosing accuracy for the simulation of the the arbitrary shaped PDN.

Acknowledgment

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Power Distribution Network Modeling for 3-D ICs with TSV Arrays

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Three-dimensional integrated circuit (3-D IC) provides a possible way to follow the prediction of Moore's Law and achieve design goals, which includes high transmission rate, low power consumption, compact size, and high integration of heterogeneous functionality. In power distribution networks (PDNs) of 3-D IC, simultaneous switching noise (SSN) will cause even more serious problems in power integrity (PI), signal integrity (SI) and electromagnetic interference (EMI) because noise coupling could occur in any direction, not just on one specific plane. To deal with these noise issues, full-wave simulation is one of the methods being adopted to accurately analyze PDNs in 3-D ICs. However, because time and memory consumption are concerned, equivalent circuit models are often used to approximate the results of full-wave simulation instead.

As shown in Fig. 1(a), PDN modeling in 3-D IC can be categorized into meshed-type PDN and via-type PDN according to the shape. Meshed-type PDN comprises power/ground grids on the chip and on the interposer, while via-type PDN includes TSVs and bumps. For the mesh-type PDN, as shown Fig. 1(b), the conventional equivalent circuits for power/ground grids are series resistance and inductance along a wire, and mutual capacitance as well as mutual inductance between two wires. For the equivalent circuit of via-type PDN, as shown in Fig. 1(c), the arrays of TSVs and bumps can be modeled similarly except for the conductivity G of silicon substrate.

In previous researches, constructing equivalent circuits of grids and TSVs separately and then combining them together is the typical modeling approach for 3-D IC PDNs. However, it assumes that there is no coupling between the power/ground grids and TSVs. In fact, the silicon substrate with low conductivity at low frequency has electrical coupling to the metals atop. This phenomenon becomes significant if the area of the metal is very large, such as high-density power/ground grids.

This coupling phenomenon can be demonstrated with a simple simulation, as shown in Fig. 2(a). A 2-D cross-section structure with two conductors in ANSYS Q2D environment, which is used to compare with the structure with two conductors located above the silicon substrate, as shown in Fig. 2(b). Since the silicon acts as a conductor at low frequency range, we can substitute it with a PEC material. The simulation results are shown in Table I. The numbers reveal that there is strong coupling between the metal and the silicon surface, but the coupling between the metals is much weaker than the case with no silicon surface Therefore, once we

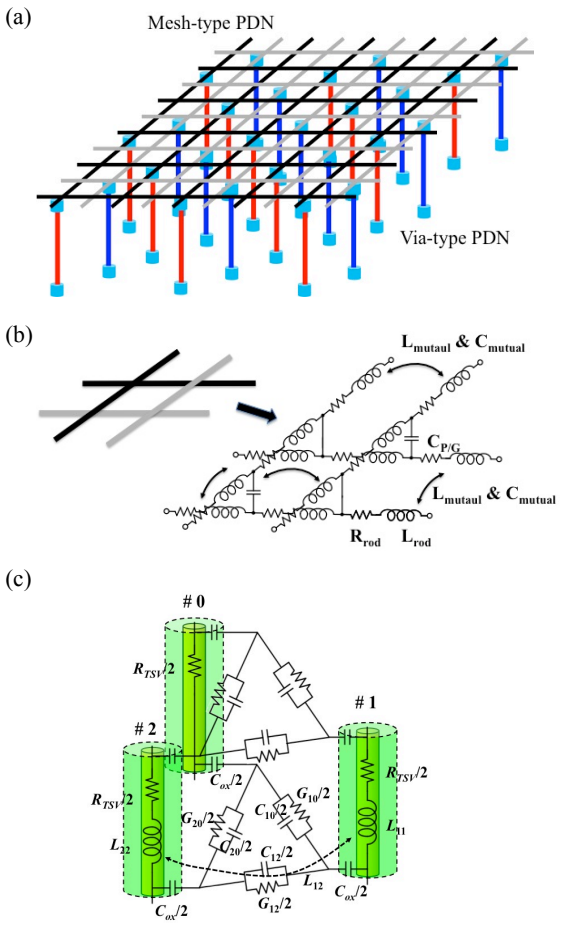

Fig. 1. Structure and equivalent circuit model of PDN in 3-D IC. (a) PDN in a 3-D IC (b) Equivalent circuit of mesh-type PDN. (c) Equivalent circuit of via-type PDN.

combine the models of power/ground grids and the TSVs together, the coupling between the metals in power/ground grids can be neglected, while only the coupling capacitances C_{m_sub} between the metals and the silicon substrate with TSVs inside need to be considered. In our case, these capacitance C_{m_sub} can be calculated approximately by the formula of microstrip line capacitance by treating the silicon surface as the ground.

The coupling node insertion method (CNIM) for array-type TSVs is proposed here to create the additional nodes for connecting the coupling capacitance C_{m_sub} between the silicon substrate and the power/ground grids. In this method, we

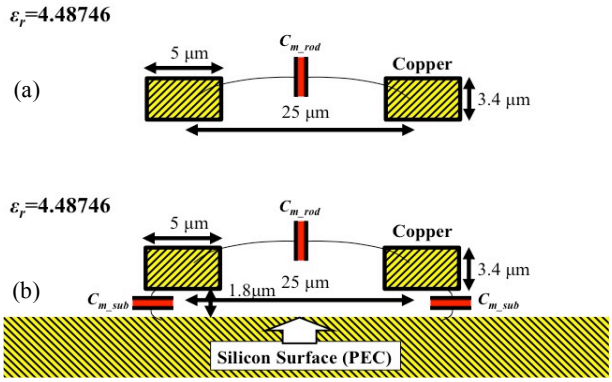

Fig. 2. Simulation for testing the effect of the silicon surface. (a) Without silicon surface. (b) With silicon surface.

TABLE I
Table for summarizing the simulation results in Fig. 2(a) and Fig. 2(b)

	Without Silicon Surface (pF/m, Fig. 4(a))	With Silicon Surface (pF/m, Fig. 4(b))
C_{m_rod}	59.412	11.496
C_{m_sub}	None	243.29

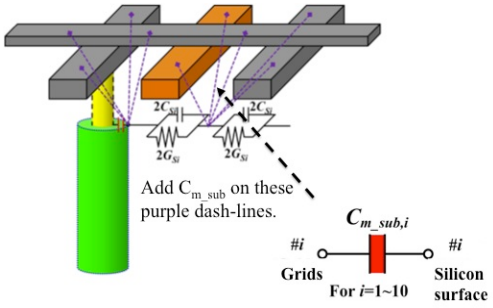

Fig. 3. The 3-D scheme for deciding where the capacitance is located between the metal and the silicon surface.

partition the Y elements of TSV model from the typical one to two series elements with each one composed of the parallel $2C_{Si}$ and $2G_{Si}$, as shown in Fig. 3. The node connected to the elements C_{ox} and C_{Si} is regarded as the silicon substrate node. On the other hand, the nodes between the R_{rod} and $L_{s,rod}$ on the power/ground grids is regarded as the metal nodes. Therefore, the two ends of the $C_{m,sub}$ elements can be connected to these nodes of the nearby TSV and power/ground grids respectively.

To demonstrate the full-PDN model and the effect of CNIM, we construct a test structure of a passive silicon interposer with metals in the redistribution layer (RDL) and connected to TSVs. As shown in Fig. 4, the test structure is composed of 16-by-16 power/ground grids on the RDL stacked on a 6-by-6 TSV array. In Fig. 4, the ports are assigned with one (Port 1) located on the power/ground grids and three (Port 2 to 4) located at the opposite end of the TSVs.

Two of numerical results for self-impedance (Z_{11}) and transfer impedance (Z_{24}) are shown in Fig. 5. The results from the full-wave simulation and the equivalent models with/without the coupling capacitances are shown in each sub-figure. The results from the equivalent model are in good

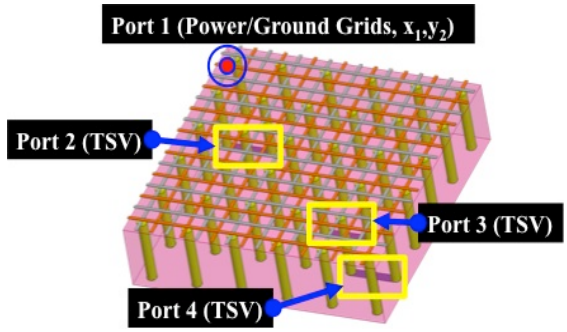

Fig. 4. Test structure for integration of mesh-type and via-type PDN and its port position.

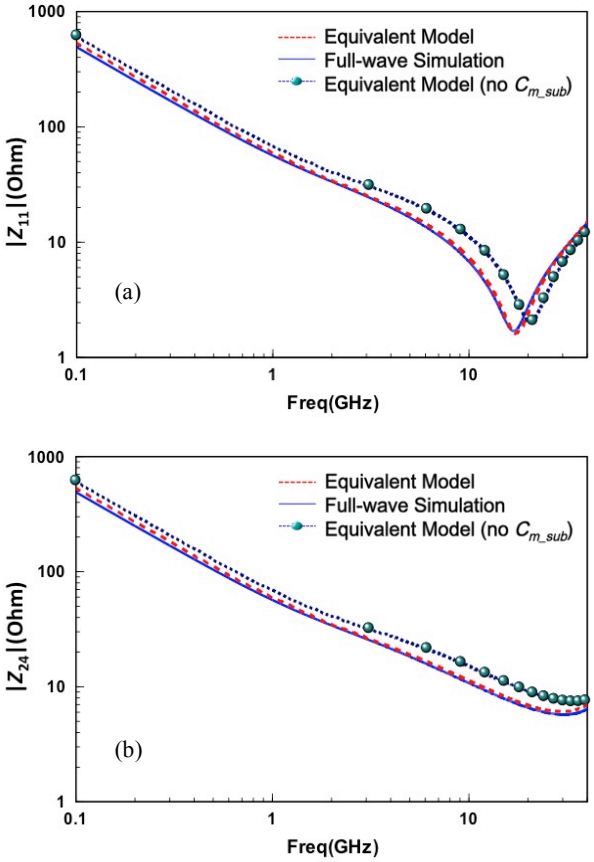

Fig. 5. Numerical results of self and transfer impedances of the test structure in Fig. 4. (a) $|Z_{11}|$. (b) $|Z_{24}|$.

consistency with full-wave simulation from DC to 40 GHz. The results shown in Fig. 7 demonstrate that considering the coupling effect using our CNIM model will greatly improve the accuracy of simulation results. Using our model, the calculated resonance frequency and magnitude of impedance are both closer to those obtained from full-wave simulator.

Therefore, the proposed CNIM can offer an effective way to revise the equivalent circuit model, obtain more accurate results in simulating PDN in 3-D IC and also lower the time and memory consumption compared with full-wave simulation.

An Explicit and Unconditionally Stable Finite Difference Scheme for the Fast Transient Analysis of a Power Distribution Network

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***Abstract*— Generally, an explicit difference scheme has the numerical stability condition which constrains the time step size, and this condition depends on the lowest reactance component. If the time step size that does not fulfill the numerical stability condition is used, unstable modes arise, and we fail the transient analysis. In this paper, we propose an explicit and unconditionally stable finite difference scheme in which the constraint of time step size is overcome by removing the unstable modes. Numerical results show that the proposed method is quite effective to perform the fast transient simulation of power distribution networks with extremely small apertures.**

I. INTRODUCTION

Significant advances of the semiconductor packaging technology have provided a complicated design of high-speed and high-density electronic circuits. Therefore, various effects depending on the high-frequency characteristics of signals cause unexpected behaviors of chips and packages on a printed circuit board. In addition, as supply voltages for these components are becoming low, the simultaneous switching noise (SSN) seriously affects the power integrity of a power distribution network (PDN). Therefore, it becomes important to verify the PDN properly in order to ensure the power integrity of the advanced packaging system.

In order to simulate the SSN by performing the circuit analysis, equivalent circuit models of the PDN are usually provided by commercially-based extractors or hand-made extraction techniques [1]. In general, if there exist fine objects or apertures in the PDN, a large number or small meshes are required for capturing the exact shapes of the fine structures. As a result, these fine meshes induce a large network and extremely small reactance elements.

There exist several explicit finite difference schemes in the circuit [2, 3] and electromagnetic simulations [4, 5] while they are basically based on primary finite difference methods [6]. These explicit schemes usually have low computational costs and can perform the fast simulations of large problems. Especially, the latency insertion method (LIM) and extended algorithms of it get considerable attention in the field of the fast transient analysis of a large-scale network [2, 3]. However, the explicit scheme has the numerical stability condition which strictly limits the maximum time step size used in the transient analysis. In order to alleviate such a numerical stability problem, the recent researches on the finite difference scheme pay much attention to unconditionally stable schemes [7, 8, 9]. Although the existing unconditionally stable schemes are more efficient than the conventional explicit method, the schemes partially include time-consuming matrix calculations.

In this paper, we propose an fully-explicit and unconditionally stable difference scheme. In the proposed method, the root cause of the instability of the explicit method is specified by using the eigenvalue decomposition. Then, the instability is eliminated by performing simple algebraic operations.

The rest of the paper is organized as follows. Section II discribes the explicit finite difference scheme in the circuit simulation and its numerical stability condition followed by the proposed explicit and unconditionally stable scheme. The accuracy and CPU time of the proposed method are verified by performing the transient simulations of the PDN with extremely-small apertures in Section III. We conclude the paper in Section IV.

II. PROPOSED METHOD

We assume that the circuit to be analysed is composed of a number of node and branch topologies shown in Fig. 1. The node topology is composed of the parallel-connected capacitor and current source, and the branch topology consists of the series-connected inductor and voltage source. By using Kirchhoff's current and voltage lows, the circuit equation associated with the network can be written in the vector-matrix form as follows

$$\mathbf{C}\frac{d}{dt}\mathbf{v} + \mathbf{M}\mathbf{i} = \mathbf{h}\,, \tag{1}$$

$$\mathbf{L}\frac{d}{dt}\mathbf{i}-\mathbf{M}^T\mathbf{v}=\mathbf{e}, \tag{2}$$

where **C** and **L** are the capacitance and inductance matrices, **v** and **i** are the voltage and current vectors, **h** and **e** are the current source and voltage source vectors, and **M** is the incidence matrix. Then, differentiating (1) with respect to time and substituting (2) into (1) lead to

$$\mathbf{C}\frac{d^2}{dt^2}\mathbf{v}+\mathbf{M}\mathbf{L}^{-1}\mathbf{M}^T\mathbf{v}=\frac{d}{dt}\mathbf{h}-\mathbf{M}\mathbf{L}^{-1}\mathbf{e}. \tag{3}$$

Equation (3) can be regarded as the second order ordinary differential equation and rewritten as

$$\mathbf{T}\frac{d^2}{dt^2}\mathbf{u}+\mathbf{S}\mathbf{u}=\mathbf{j}, \tag{4}$$

where

$$\mathbf{T}=\mathbf{C}, \tag{5}$$

$$\mathbf{S}=\mathbf{M}\mathbf{L}^{-1}\mathbf{M}^T, \tag{6}$$

$$\mathbf{u}=\mathbf{v}, \tag{7}$$

$$\mathbf{j}=\frac{d}{dt}\mathbf{h}-\mathbf{M}\mathbf{L}^{-1}\mathbf{e}, \tag{8}$$

T is the $N\times N$ symmetric positive definite matrix, **S** is the $N\times N$ positive semidefinite matrix, **u** is the unknown vector, and **j** is the current excitation vector. The generalized eigenvalue problem related to (4) is written in the following form [10]

$$\mathbf{S}\boldsymbol{\varphi}=\lambda\,\mathbf{T}\boldsymbol{\varphi}. \tag{9}$$

In this case, N eigenvalues $(\lambda_1,\lambda_2,...,\lambda_N)$ and corresponding eigenvectors $\boldsymbol{\varphi}$ can be obtained by solving (9). By defining the matrix $\boldsymbol{\Phi}=[\boldsymbol{\varphi}_1\ \boldsymbol{\varphi}_2\ ...\ \boldsymbol{\varphi}_N]$, which stores the N eigenvectors in its colmuns, and premultiplying both sides of (4) by $\boldsymbol{\Phi}^T$, (4) can be rewritten as

$$\frac{d^2}{dt^2}\mathbf{y}+\mathbf{D}\mathbf{y}=\boldsymbol{\Phi}^T\mathbf{j}, \tag{10}$$

where $\mathbf{u}=\boldsymbol{\Phi}\mathbf{y}$, $\boldsymbol{\Phi}^T\mathbf{T}\boldsymbol{\Phi}=\mathbf{I}$ [11], **I** is the unit matrix, $\mathbf{D}=\boldsymbol{\Phi}^T\mathbf{S}\boldsymbol{\Phi}=diag\{\lambda_1,\lambda_2,...,\lambda_N\}$, $diag\{\cdot\}$ denotes a diagonal matrix, and λ_i and $\boldsymbol{\varphi}_i$ $(i=1,2,...,N)$ are the i-th eigenvalue and eigenvector, respectively. Additionally, **y** is the unknown coefficient vector which is derived by projecting **u** on the eigenspace $\boldsymbol{\Phi}$, and $\boldsymbol{\varphi}_i$ corresponds to each mode obtained by the mode decomposition of (4) [10]. Applying the explicit central-difference scheme to (10) and rearranging the equation lead to the following updating formula of **y**

$$\mathbf{y}^{n+1}=2\mathbf{y}^n-\mathbf{y}^{n-1}-\Delta t^2\mathbf{D}\mathbf{y}^n+\Delta t^2\boldsymbol{\Phi}^T\mathbf{j}, \tag{11}$$

where n is the time index, and Δt is the time step size. In this case, Δt must fulfill the numerical stability condition [10],

$$\Delta t^2\lambda_i^2\le 4,\quad i=1,2,...,N. \tag{12}$$

Because $\sqrt{\lambda_i}$ is an angular resonance frequency associated with (4), if high-frequency components are contained in the numerical solutions, Δt becomes a very small value. Therefore, the calculation cost increases dramatically, and the above explicit method is not effective especially for the simulation of the object which has extremely fine structures.

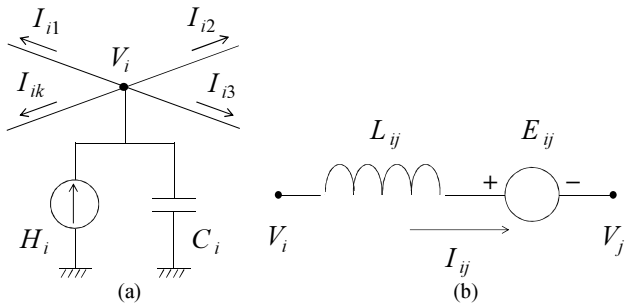

Fig. 1. The network topologies constituting the lossless network. The arrows correspond to the directions of the branch currents. (a) Node topology. (b) Branch topology.

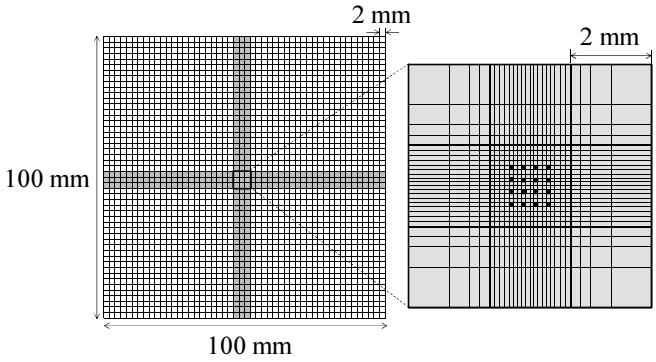

Fig. 2. The rectangular meshes of the PDN with extremely fine apertures. The gray cells have rectangular shape, and the black ones represent the apertures. (a) The top-view. (b) The closeup of the central part.

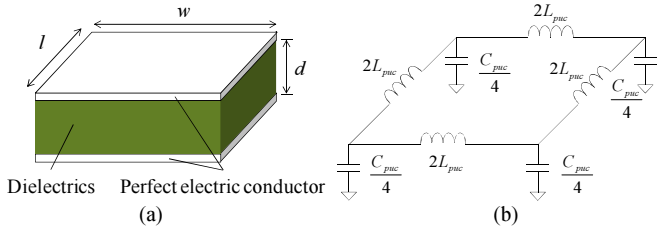

Fig. 3. The unit-cell constituting the PDN. (a) The unit-cell and (b) its Pi-type equivalent circuit.

In the proposed method, the explicit updating formula (11) is improved as follows: First, in order to obtain the accurate numerical solutions in the transient analysis, we make include the component related to not less than ten times higher frequency than the maximum one, $f_{\max}$, into the solutions. To do so, the time step size Δt has to be satisfied with

$$\Delta t\le\Delta\widetilde{t}_{\max}=\frac{1}{10}f_{\max}. \tag{13}$$

Next, in the case that $\Delta t=\Delta\widetilde{t}_{\max}$, the eigenvectors stored in $\boldsymbol{\Phi}$ are divided into two groups, namely, $\boldsymbol{\Phi}_l$ and $\boldsymbol{\Phi}_h$ so that $\boldsymbol{\Phi}=[\boldsymbol{\Phi}_l\ \boldsymbol{\Phi}_h]$: eigenvalues associated with the eigenvectors in $\boldsymbol{\Phi}_h$ do not fulfil (12), whereas those associated with $\boldsymbol{\Phi}_l$ do. The unknowns in **y** are also divided into two groups related to $\boldsymbol{\Phi}_l$ and $\boldsymbol{\Phi}_h$ so that $\mathbf{y}=[\mathbf{y}_l^T\ \mathbf{y}_h^T]^T$. In other words, we categorize the stable modes as $\boldsymbol{\Phi}_l$ and the unstable modes as

$\mathbf{\Phi}_h$. Then, removing the unstable modes $\mathbf{\Phi}_h$ and redefining $\mathbf{\Phi}$ and $\mathbf{y}$ so that $\mathbf{\Phi} = \mathbf{\Phi}_l$ and $\mathbf{y} = \mathbf{y}_l$ lead to the stable and explicit updating formulation in the form of (11). the numerical solutions obtained from the proposed updating formula are calculated stably without the direct matrix operations even if $\Delta\tilde{t}_{\max}$ is used.

III. Numerical Results

The PDN illustrated in Fig. 2 is analysed to verify the accuracy and efficiency of the proposed method. The PDN is composed of the parallel perfect electric conductor planes and FR4 between the planes. The size of the PDN is 100 mm $\times$ 100 mm, and the thickness of FR4 is 0.5 mm. Since 16 square apertures, each of which is 0.2 mm on a side, exist on the central part of the PDN, the narrower grid spacing than that in the other part is used around the apertures. The relative permittivity of FR4 is $\varepsilon_r = 4.0$. In this example, we assume that the maximum frequency $f_{\max} = 5.0\,\text{GHz}$, and the wave propagation speed $c_r = 1.5\times10^8$ m/s in the media, and the minimum wavelength becomes 30 mm. To perform accurate simulations, the maximum cell size is set to 2.0 mm, which is less than one-tenth of the wavelength. Since the apertures are extremely small compared to the PDN, the low reactance components are produced. As a result, the PDN is divided using nonuniform rectangular meshes into 65×65 unit cells, one of which is shown in Fig. 3(a). The unit cell is modeled as the Pi-type equivalent circuit illustrated in Fig. 3(b). In our case, the per-unit-cell inductance L_{puc} and capacitance C_{puc} in the Pi-model are calculated as follows:

$$L_{puc} = \mu_0 \frac{dl}{w}, \tag{14}$$

$$C_{puc} = \varepsilon_0 \varepsilon_r \frac{wl}{d}, \tag{15}$$

where μ_0 and ε_0 are the permeability and permittivity of the vacuum, l is the cell length, w is the cell width, and d is the distance between the planes. The number of the nodes of the equivalent circuit is 4221, and therefore, 4221 eigenvalues are calculated from **S** and **T**. Fig. 5 shows the time step sizes, each of which is the maximum value satisfying (12) and related to the eigenvalue λ_i. According to (13) and $f_{\max}$, the time step size $\Delta\tilde{t}_{\max}$ is calculated to 20 ps and shown as the dot-dashed line in Fig. 5. Clearly, 3813 time step sizes are less than $\Delta\tilde{t}_{\max}$, and therefore, the unstable modes arise if $\Delta\tilde{t}_{\max}$ is used in the existing explicit scheme. As a result, the existing scheme has to use the minimum time step size $\Delta t_1 = 0.9\,\text{ps}$, which increases the computational cost of the transient simulation. These very small time step sizes come from low reactance components in the equivalent circuit related to the extremely fine structures in the computational domain, namely, PDN. On the other hand, by removing the unstable modes, $\Delta\tilde{t}_{\max}$, which is about 20 times larger than $\Delta\tilde{t}_1$, can be used in the proposed method. A current source is appended to the node at the bottom-left corner of the PDN as an input excitation. The input has the triangular waveform of which the rise and fall times are 1 ns, the amplitude is 0.01 A. We perform the transient analysis by using the proposed method, LIM, and HSPICE.

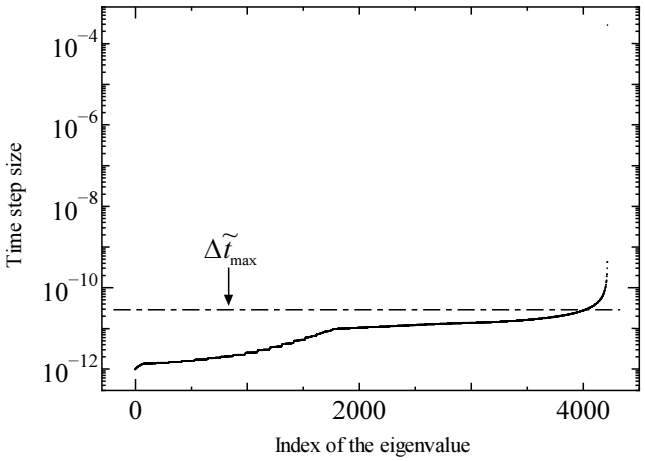

Fig. 4. Index of the eigenvalue versus time step size Δt_i.

Figs. 5, 6, and 7 show the voltage waveforms at the top-right corner obtained by setting the time step size to 0.9 ps or 20 ps. In these figures, the waveform obtained using HSPICE with the time step size of 1 ps is shown as *Reference*. As illustrated in Fig. 5, the waveform of HSPICE changes with the time step size except for the case of 1 ps, and the reference waveform agrees with that obtained from the LIM. Therefore, we regard the reference waveform as the most accurate one in this verification. From Fig. 6, we can see that the waveform of the proposed method with 0.9 ps time step size completely agrees with the reference waveform. In addition, in Fig. 7, the proposed method can provide the numerically stable solutions with appropriate accuracy even if 20 ps is used. Table I shows the CPU time in the case that the simulation interval is from 0 ns to 100 ns and the speed-up ratio between HSPICE with $\Delta\tilde{t}_{\max}$ = 20 ps and the other methods. From Table I, the proposed method is about 1048 times faster than the LIM and about 21462 times faster than HSPICE. As a result, it is confirmed that the proposed method is as accurate as the conventional solvers and much more efficient than them in the simulation of the PDN with the extremely-small apertures.

IV. Conclusion

In this paper, we have proposed the method which can overcome the time step size limitation of the existing explicit difference scheme by removing the unstable modes. The unstable modes were specified by using the eigenvalue decomposition and defining the maximum frequency of interest. The numerical results showed that the proposed method was comparable to the LIM and HSPICE from a viewpoint of the accuracy. In addition, it has been confirmed that our approach was much faster than HSPICE and could reduce the computational cost of the existing scheme effectively.

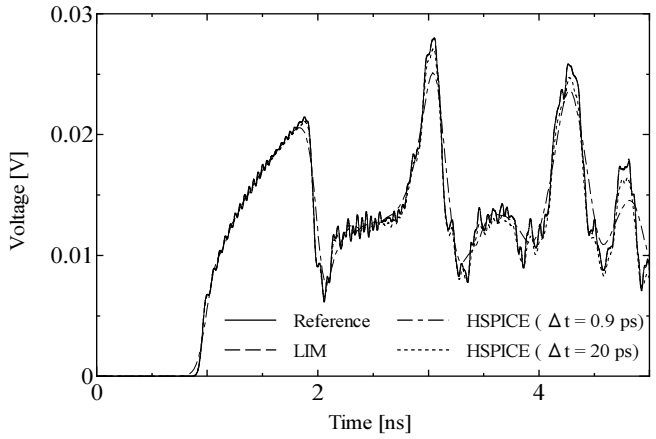

Fig. 5. Comparison of the voltage waveforms between HSPICE and LIM.

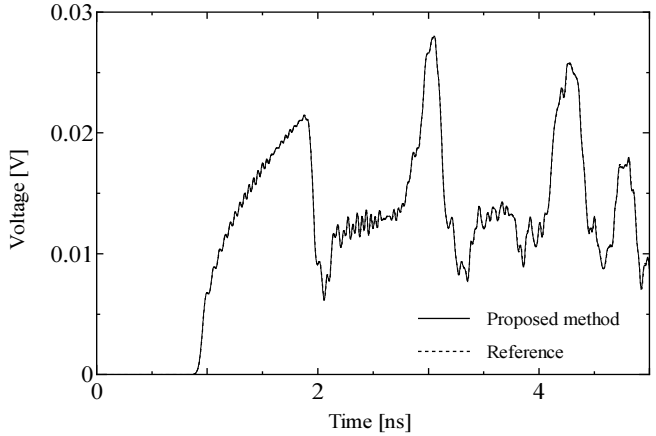

Fig.6. Voltage waveforms in the case that $\Delta t = 0.9$ ps.

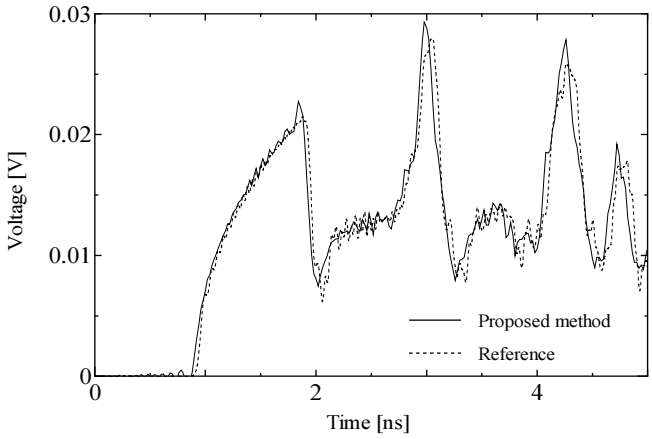

Fig.7. Voltage waveforms in the case that $\Delta t = 20$ ps.

TABLE 1

CPU TIME

Method	Δt (ps)	CPU time (ms)	Speed-up
Proposed	0.9	3140	109
	20	16	21462
LIM	0.9	16765	20
	20	N/A	N/A
HSPICE	0.9	8143530	0.04
	20	343390	1

ACKNOWLEDGMENT

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Fast Transient Analysis of Multiconductor Transmission Lines Using Nodal Block Relaxation (NBR) Method

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***Abstract*— This paper describes a nodal block relaxation (NBR) method in which the block relaxation method is applied to the nodal circuit equation restructured from the modified nodal equation. First, the circuit equation formulated by the RLCG-MNA method is transformed into the nodal equation composed of only node voltage variables. As a result, the block relaxation method becomes available in the numerical solutions of tightly coupled multiconductor transmission lines. Finally, numerical results show that the proposed method is efficient for the fast simulation of multiconductor transmission lines.**

I. INTRODUCTION

In order to estimate signal delay, reflection, and cross-talk on tightly coupled multiconductor transmission lines (MTLs), circuit-based modeling and simulation techniques are adequate in terms of accuracy and efficiency. Although general-purpose SPICE-like simulators are applicable to such a simulation, their algorithms with sparse matrix techniques are not efficient in the transient analysis of a coupled network. Recently, the block latency insertion method (block-LIM) has been proposed for the fast simulation of the MTLs, but it has a strict numerical stability condition, which may reduce the efficiency of the block-LIM significantly [1]. On the other hand, the nodal analysis (NA) approach used in [2] is useful for the simulation of interconnects because it eliminates the current variables so that only the node voltages are variables in a circuit equation. However, the NA approach has not been applied to the coupled network explicitly.

In this paper, we apply the NA approach to the equivalent circuit of the MTLs along with the block-relaxation method. The nodal block relaxation (NBR) method enables to exploit several times larger time step size than that of the block-LIM and works effectively to separate locally dense parts in the MTLs. And its iterative solution converges rapidly due to the positive definite coefficient matrix of the circuit equation obtained by the NA formulation. The algorithm of the proposed method is similar to the block-LIM, but it has superior features related to the numerical stability and convergence.

The remainder part of the paper is organized as follows. In Section II, we begin with the RLCG-MNA formulation and generate the iterative updating formula of the proposed method by combining the NA approach and block relaxation method. Section III shows some numerical results, and the conclusion is given in Section IV.

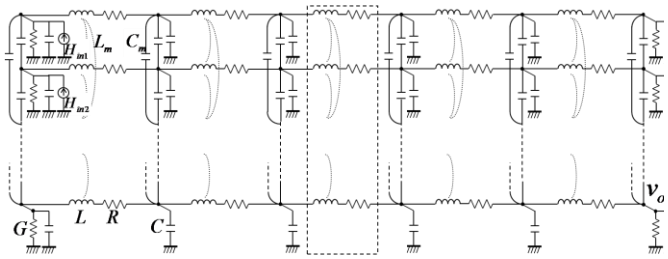

Fig. 1. The equivalent circuit of MTLs which is composed of 128 transmission lines.

II. THE PROPOSED METHOD

The equivalent circuit of the MTLs is shown in Fig. 1. To derive the circuit equation associated with the network in Fig. 1, we first apply the RLCG-MNA method [3] to the circuit. The RLCG-MNA method can generate a low-dimensional circuit equation by eliminating the node voltage variable corresponding to the intermediate node in every resistor-inductor series-connected branch as follows.

$$\begin{bmatrix} \mathbf{G} & \mathbf{M} \\ -\mathbf{M}^{\mathrm{T}} & \mathbf{R} \end{bmatrix} \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix} + \begin{bmatrix} \mathbf{C} & \mathbf{0} \\ \mathbf{0} & \mathbf{L} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix} = \begin{bmatrix} \mathbf{h} \\ \mathbf{e} \end{bmatrix}, \qquad (1)$$

where **v**, **i**, **h**, and **e** are the node voltage, branch current, independent current source, and independent voltage source vectors, and **R**, **L**, **C**, and **G** are the resistance, inductance, capacitance, and conductance matrices. The matrix **M** is the incidence matrix which represents the relation of connection between the voltages and currents.

In the next step, applying the backward difference method at the (n+1)-th step to (1) leads to

$$\begin{bmatrix} \frac{1}{\Delta t}\mathbf{C}+\mathbf{G} & \mathbf{M} \\ -\mathbf{M}^{\mathrm{T}} & \frac{1}{\Delta t}\mathbf{L}+\mathbf{R} \end{bmatrix} \begin{bmatrix} \mathbf{v}^{n+1} \\ \mathbf{i}^{n+1} \end{bmatrix} = \begin{bmatrix} \frac{1}{\Delta t}\mathbf{C} & \mathbf{0} \\ \mathbf{0} & \frac{1}{\Delta t}\mathbf{L} \end{bmatrix} \begin{bmatrix} \mathbf{v}^{n} \\ \mathbf{i}^{n} \end{bmatrix} + \begin{bmatrix} \mathbf{h}^{n+1} \\ \mathbf{e}^{n+1} \end{bmatrix}, \qquad (2)$$

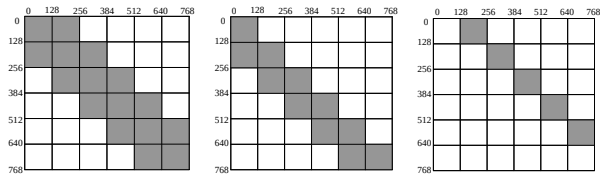

Fig. 2. Structural representations of coefficient matrices. (a) **T** in (5). (b) **P** in (6). (c) **Q** in (6).

where Δt is the time step size, and n denotes the time step. In this case, because the coefficient matrix in the left-hand side of (2) is not a positive definite matrix, it is not suitable for a relaxation-based numerical simulation.

In order to overcome this drawback, we follow the NA approach: First, (2) is partitioned into two equations

$$\left(\frac{1}{\Delta t}\mathbf{C}+\mathbf{G}\right)\mathbf{v}^{n+1}+\mathbf{M}\mathbf{i}^{n+1}=\frac{1}{\Delta t}\mathbf{C}\mathbf{v}^{n}+\mathbf{h}^{n+1}, \tag{3}$$

$$-\mathbf{M}^{\mathrm{T}}\mathbf{v}^{n+1}+\left(\frac{1}{\Delta t}\mathbf{L}+\mathbf{R}\right)\mathbf{i}^{n+1}=\frac{1}{\Delta t}\mathbf{L}\mathbf{i}^{n}+\mathbf{e}^{n+1}. \tag{4}$$

Next, eliminating $\mathbf{i}^{n+1}$ from (3) by using (4) leads to

$$\mathbf{T}\mathbf{v}^{n+1}=\frac{1}{\Delta t}\mathbf{C}\mathbf{v}^{n}-\mathbf{M}\hat{\mathbf{K}}\frac{1}{\Delta t}\mathbf{L}\mathbf{i}^{n}+\mathbf{s}, \tag{5}$$

where

$$\mathbf{T}=\frac{1}{\Delta t}\mathbf{C}+\mathbf{G}+\mathbf{M}\hat{\mathbf{K}}\mathbf{M}^{\mathrm{T}},\quad \hat{\mathbf{K}}=\left(\frac{1}{\Delta t}\mathbf{L}+\mathbf{R}\right)^{-1},\quad \mathbf{s}=\mathbf{h}^{n+1}-\mathbf{M}\hat{\mathbf{K}}\mathbf{e}^{n+1}.$$

The coefficient matrix **T** in (5) is shown in Fig. 2(a), and we can see that **T** is a block tridiagonal matrix. Furthermore, it can be proven that **T** is the symmetric positive definite matrix, and therefore, the convergence of the block relaxation method is guaranteed. Subsequently, in order to apply the block relaxation method to (5), **T** is split into the block lower triangular matrix **P** and upper triangular matrix **Q** as shown in Fig. 2(b) and (c). Then the iterative updating formula is obtained and written as

$$\mathbf{P}\mathbf{v}^{n+1,(k+1)}=-\mathbf{Q}\mathbf{v}^{n+1,(k)}+\frac{1}{\Delta t}\mathbf{C}\mathbf{v}^{n}-\mathbf{M}\hat{\mathbf{K}}\frac{1}{\Delta t}\mathbf{L}\mathbf{i}^{n}+\mathbf{s}, \tag{6}$$

where k is the iteration counter. As described above, because **T** generated by the NA approach is the symmetric positive definite matrix, **T** ensures the convergence of the iterative solutions. After updating the node voltages, the unknown current variables are updated by using (4).

III. Numerical Results

We perform the transient analyses of the circuit shown in Fig. 1 by using the proposed method and block-LIM. We set the element values as follows: R = 100 Ω, L = 1.0 nH, C = 0.01 pF, G = 0.02 S, L_m = 0.03 nH, and C_m = 1.0 fF, where L_m and C_m are the mutual inductance and mutual capacitance. Furthermore, that we use L/100 and L_m/100 as the inductance and mutual inductance within the dotted rectangle in Fig. 1. The input current sources H_{in1} and H_{in2} are trapezoidal pulses. These sources are the same trapezoidal pulse of which the initial value is 0 A, pulse value is 0.02 A, rise and fall times are 0.2 ns, pulse width is 1.0 ns and period is 2.2 ns, except for the delay times, which are 0.5 ns and 0.6 ns, respectively. The number of the iterations used in the proposed method is fixed and equal to N_k. The simulation interval is from 0 ns to 4.5 ns.

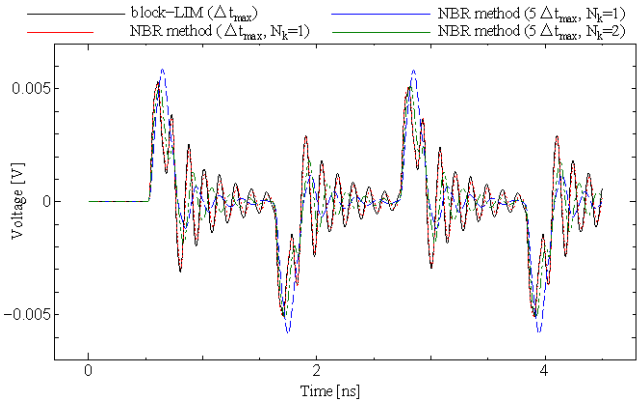

Fig. 3. Waveform results of v_{obs}.

TABLE I
COMPARISON OF CPU TIME

Method	CPU time (s)	Speedup
block-LIM ($\Delta t_{\max}$)	38.44	1.00
Proposed method ($\Delta t_{\max}$, N_k=1)	45.29	0.85
Proposed method ($5\Delta t_{\max}$, N_k=1)	9.11	4.21
Proposed method ($5\Delta t_{\max}$, N_k=2)	11.44	3.36

The waveform results of v_{obs} are illustrated in Fig. (3), where $\Delta t_{\max}$ is the maximum time step size used in the block-LIM. In Fig. 3, it is confirmed that the waveform results of the proposed method are numerically stable and agree with that of the block-LIM. The CPU times and speed-up ratios to the block-LIM are shown in Table I. In Table I, it is confirmed that the proposed method with $5\Delta t_{\max}$ and N_k = 2 is about 3.36 times faster than the block-LIM without losing accuracy. Note that the proposed method is substantially fast because the block-LIM itself is more than ten times faster than HSPICE.

IV. Conclusion

In this paper, we have proposed the efficient circuit simulation technique, NBR, based on the NA approach and block relaxation method. In the proposed method, the low-dimensional circuit equation was generated by combining the RLCG-MNA method and the NA approach. Finally, NBR method was applied to solve the resultant equation. Numerical results showed that the proposed method was

about 3.36 times faster than the block-LIM with appropriate accuracy.

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A Novel Broadband Bandstop Filter Design

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***Abstract*—A novel wide stopband and compact bandstop filter (BSF) is proposed and realized based on defected ground structure (DGS) and meandered signal line. A condition for transmission zeros is derived. It can be observed that the equivalent circuit model reasonably agrees with the full-wave simulation and measurement results. Also, it is found that the proposed filter has high rejection over 25 dB in its stopband. The filter has a compact size of 0.21 λ_g × 0.19 λ_g, where λ_g is the wavelength of the center frequency of the stopband, and its -10 dB fractional bandwidth (FBW) is up to 90%.**

Keywords- Bandstop filter (BSF); defected ground structure (DGS).

I. INTRODUCTION

Defected ground structure (DGS) has been widely used in microwave and millimeter wave circuits recently for size reduction. It is realized by etching defects on the ground plane. The function of DGS is that the defect can disturb return currents, which results in additional inductance and capacitance to create resonance at some frequency. The resonance property provides a band-rejection characteristic, which can be directly used in designing BSFs.

Several approaches [1]-[9] have been proposed for BSF design based on DGS. Conventional DGS has the shape of dumbbell [1] or spiral [2]. Later on, various shapes have been brought out and discussed, such as UV slots [3], double-H shaped [4], modified dumbbell shaped [5], T shaped [6], E shaped [7], and modified-E shaped [8]. However, the common problem of [1]-[8] is that only one transmission zero (TZ) is generated by a unit cell, which in turn results in narrow stopband bandwidth of BSF. To achieve a wider stopband, one method is cascading several unit cells, like three cascaded V-slots DGS in [3], which is at the expense of occupying larger surface area. On the other hand, double equilateral U shaped DGS in [9] can generate two TZs. Nevertheless, the rejection between two TZ is not high; therefore, if -10 dB rejection is required, the unit cell in [9] still cannot create a wide stopband.

In this paper, a novel BSF is proposed by using a DGS and meandered signal line. The proposed BSF can generate more than one TZ to achieve wide stopband. In addition, the corresponding equivalent circuit model is constructed and analyzed, and the TZs condition is derived and discussed. Finally, a test sample is designed and fabricated. The surface area of the proposed BSF is 7.6 mm × 6.9 mm, which is small. It is only 0.04 λ_g^2, in terms of the wavelength propagating in the substrate. Besides, it has a wide stopband, which covers from 2.24 GHz to 5.93 GHz below -10 dB, and possesses a large FBW equal to 90% by measurement.

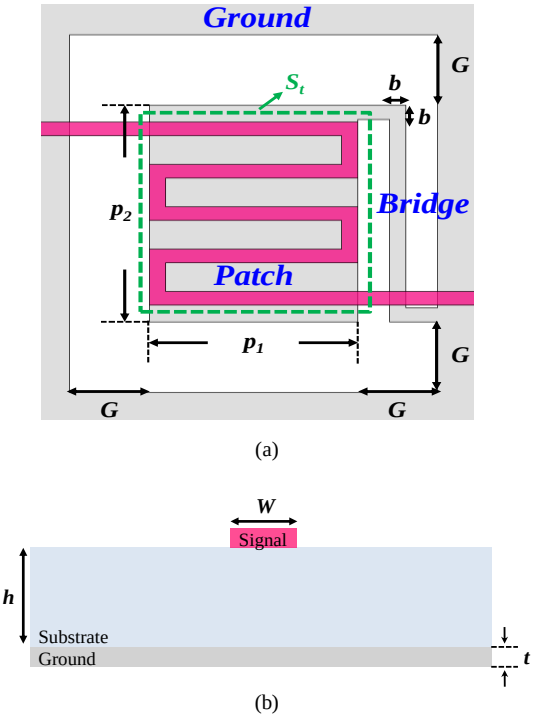

Figure 1. The proposed BSF: (a) Top view (b) Side view

II. STRUCTURE AND DESIGN CONCEPT

The proposed BSF is implemented in a two-layered structure, and its top view and side view are shown in Figs.

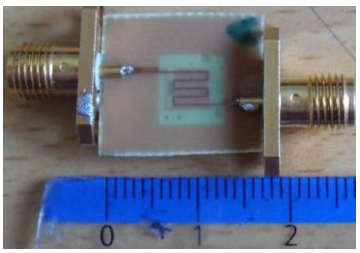

Figure 2. Test sample of the proposed BSF

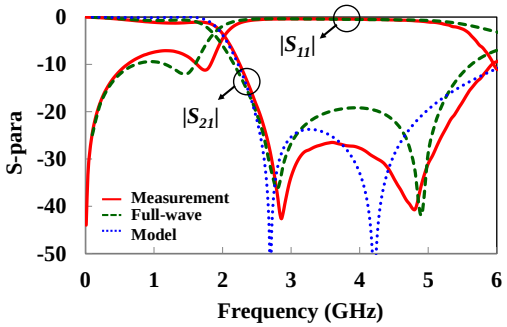

Figure 3. Return loss and insertion loss of the proposed BSF.

1(a) and (b). As can be shown in Fig. 1(a), the filter comprises a meandered signal trace on the top layer, and a ground plane with DGS on the bottom layer. The DGS is composed of two parts, one is Bridge, and the other is Patch. Bridge is a connection of Ground and Patch, and the width of bridge is denoted as *b*. On the other hand, Patch is a floating ground with slots surrounded, and p_1, p_2 are used to describe the size of Patch, and *G* is the gap between Patch and Ground. In addition, total length of the meandered signal line, line width, substrate height and metal thickness are denoted as S_t, *W*, *h*, and *t*, respectively.

As we know, multiple TZs can produce a wide stopband; therefore, it is essential to know how TZs are introduced by the proposed filter. The TZ condition is derived as follows:

$$1-4\pi^2 L_{DGS} C_{DGS} f_Z^{\,2} = \frac{2\pi}{Z_M}(L_{DGS} - L_m)\sin E_M \cdot f_Z \,. \quad (1)$$

III. Simulation and Measurement

A BSF test sample is fabricated with FR4 substrate and occupies an area of 7.6 mm × 6.9 mm, as shown in Fig. 2. The dielectric constant is 4.3, and the loss tangent is 0.02. Fig. 3 displays the return loss and the insertion loss of measurement results and simulation results (full-wave and equivalent circuit model), respectively. Good agreement between measurement results and full-wave simulation is observed. The cutoff frequency is defined by -10 dB, and a wide stopband from 2.24 GHz to 5.93 GHz for measurement can be observed in Fig. 3.

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A Solution and Its Estimation Method for Slot-crossing Signals to Reduce ISI-increased Crosstalk

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***Abstract*—A branched reflector technique for the suppression of slot-induced crosstalk especially including the effect of inter-symbol interference (ISI) is newly proposed. A fast algorithm for the performance evaluation of the proposed technique is also provided. To fulfil this algorithm, a flow chart is suggested to quickly estimate the slot-induced crosstalk for arbitrary system excitation with any operating speed. Further, the estimated results obtained are compared with the measured ones. Good agreement between them confirms the validity of the proposed algorithm. Also, the effectiveness of the proposed technique is well demonstrated based on these obtained results.**

I. INTRODUCTION

In order to satisfy the demand for high performance, low-cost and compact electronic products nowadays, more and more highly integrated multi-chip modules (MCM), system-in-a-packages (SIP), and high-density printed circuit boards (PCB) are employed in design. For such, the isolation of power/ground noise and the separation of different voltage supplies related to different chips become critical. Splitting power/ground planes has been verified to be an effective and low-cost solution to these problems [1], [2]. However, high-speed signal lines sometimes unavoidably cross the slotted power/ground planes under high-density routing. Many signal-integrity issues such as reflection, crosstalk, and radiated emission thus arise [3]-[5].

Many solutions have been proposed to reduce the slot-induced crosstalk stated above. The most commonly used method is to add stitching capacitors [5], which can provide a return current path at high frequency range and still maintain the isolation between the split power/ground planes at the direct current (DC) level. However, these additional capacitors increase the fabrication cost. Furthermore, the effective series inductance (ESL) of the component-type capacitor invalidates the capacitor at high frequency range and the potential LC resonance may result in longer duration of crosstalk.

Recently, a branched reflector technique for slot-induced crosstalk suppression has been proposed [6]. Its physical mechanism and design method have been investigated only for the step input source; nevertheless, the crosstalk may be highly increased due to the inter-symbol interference (ISI). In this paper, the design method of branched reflector technique is refined and able to reduce the slot-induced crosstalk especially increased by the ISI effect, for which the pseudo random bit sequence (PRBS) is considered as the input source. To estimate this performance, a new fast algorithm evolved from the previous one [7] and its flow chart are also proposed. This new algorithm can take the ISI effect into account and rapidly assess the crosstalk for arbitrary system excitation with any operating speed.

II. PROPOSED TECHNIQUE AND ESTIMATION METHOD

A. Proposed Solution and Its Equivalent Circuit Model

Fig. 1(a) shows the physical structure of the solution board with a branched reflector. On the top layer, two identical microstrip lines with length $2 \cdot L_2$ and width W_m are printed. The distance between these two lines is $2 \cdot L_{s2}$. The bottom layer is a ground plane. A slot line with width W_s is etched in the middle of this plane and both ends of the slot line are kept a distance L_1 to the plane edges. The spacing between each end of the slot line and its adjacent microstrip line is L_{s1}. An open stub with width W_{br} and length L_{br} is printed on the top layer and connected to the ground plane by a via in the center of the two lines. This open stub is called branched reflector hereafter. The branched reflector can highly decrease the slot-induced crosstalk if L_{br} and W_{br} are properly designed [6].

Fig. 1(b) shows the equivalent circuit model of the structure shown in Fig. 1(a). In this model, the characteristic impedance of each microstrip line is represented by Z_m. For simplicity, the frequency-dependant characteristic impedance of the slot line is assumed to be a constant Z_s while the characteristic impedance of the branched reflector is Z_{br}. From this equivalent circuit model, it can be easily observed that the slot-induced near-end and far-end crosstalk are identical in magnitude. Therefore, only the near-end crosstalk will be considered in the following sections.

B. Brief Introduction for Algorithm

The first step of the proposed algorithm is to obtain the step response of the considered system. This response can be used to rapidly predict the maximum ISI-increased crosstalk incorporating with the following steps of this algorithm. Once the step response is obtained, the maximum crosstalk voltage (V_{max}) for the PRBS input with a specific bit-rate can be calculated as [7]

$$V_{\max} = \max_n \{V_{\max,n}\}, \tag{1}$$

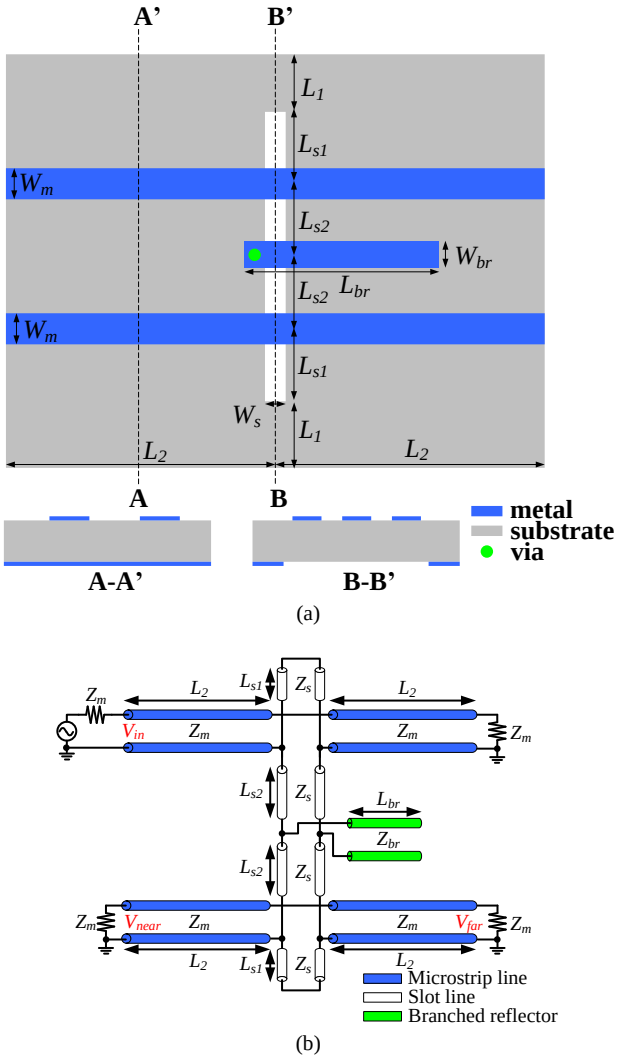


Fig. 1. The proposed structure: (a) its top and side views, and (b) its corresponding equivalent circuit model.

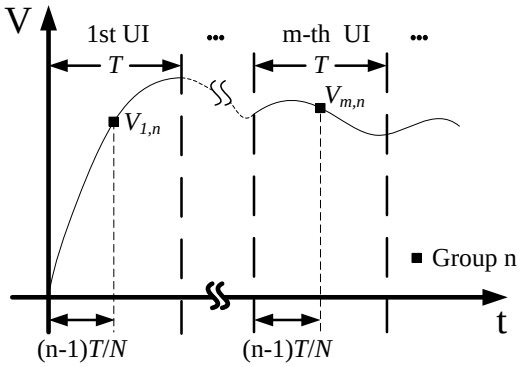


Fig. 2. A typical step response.

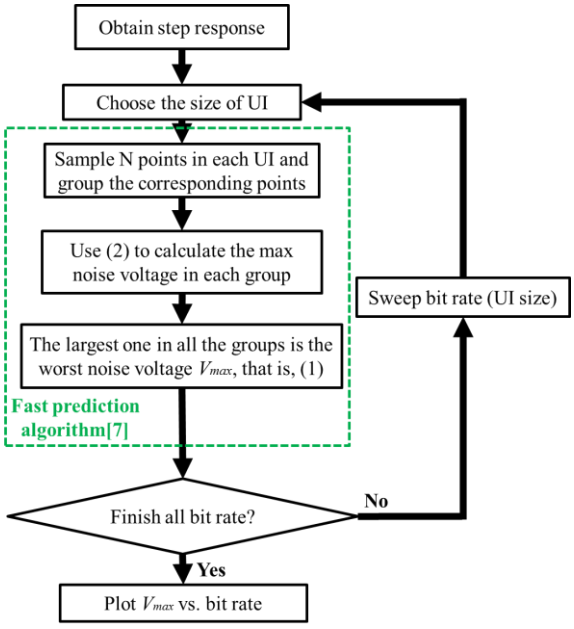


Fig. 3. The flow chart of the proposed algorithm.

where $V_{max,n}$ denotes the maximum voltage of the group n (see Fig. 2) and can be expressed as

$$V_{\max,n} = \sum_i M_{i,n} - \sum_j m_{j,n}. \quad (2)$$

In Fig. 2, $M_{i,n}$ denotes the i^{th} local maximum voltage in the set of group n, while $m_{j,n}$ denotes the j^{th} local minimum voltage in the same set. The duration of each unit interval (UI) is denoted as T and the number of the sampling points in each UI is represented by N.

Fig. 3 shows the flow chart of the proposed algorithm. In this chart, three steps surrounded by a dashed line are suggested by the previous research [7]. According to this chart, many steps are essential to fast and successful estimation of the ISI-increased crosstalk for arbitrary system excitation with any operating speed. First, the step response of the crosstalk for the system can be obtained by circuit simulation or even measurement. Second, the UI size is determined by the operating bit-rate of the system. Then, (1) and (2) can be applied to get the maximum crosstalk with respect to the given step response. Third, if there is any other bit rate in the interested range, the iterating procedure proceeds with the UI size changed. It is worth mentioning that by using this algorithm, the influence of ISI-increased crosstalk with different operating speed can be well evaluated without running the time-consuming simulation for step response again. Furthermore, it provides a straightforward assessment for efficiently analyzing the proposed technique.

III. Prediction of Worst ISI-increased Crosstalk

In this section, the effectiveness of the proposed technique and its evaluation following the algorithm as described in Part B of Section II will be well verified. Then, some important properties related to this technique will be revealed.

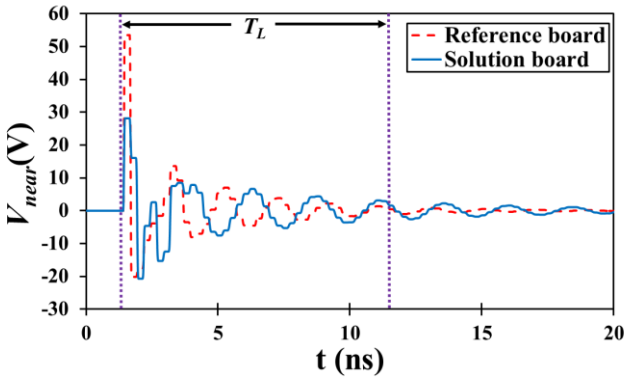
A. Numerical Result

Table I summarizes the physical dimension of the proposed structure (see Fig. 1(a)), which would be viewed as a solution board for demonstration. The reference board without the branched reflector has the same dimension as the solution

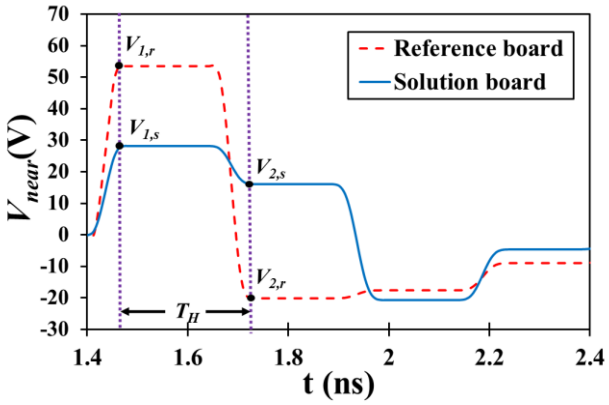
TABLE I

THE VALUES OF STRUCTURE PARAMETERS

Variable	Length (mm)	Variable	Length (mm)
L_1	25	L_{br}	20
L_{s1}	25	W_m	1.5
L_{s2}	75	W_s	1
L_2	50	W_{br}	1.5



(a)



(b)

Fig. 4. The near-end crosstalk: (a) the whole waveform, and (b) the enlarged partial waveform.

board. The equivalent circuit model in Fig. 1(b) would be used to obtain the required step response. The characteristic impedances for Z_m, Z_s, and Z_{br} are 50 Ω, 90 Ω, and 50 Ω, respectively. A step voltage source (V_s) with a magnitude of 0.5 V is connected to the input end of the upper microstrip line and the circuit simulator [8] is used for the time-domain simulation. Fig. 4(a) shows the step response of the near-end crosstalk (V_{near}) for the solution and reference boards, and Fig. 4(b) illustrates the zoom-in view of Fig. 4 (a). Then, these two step responses could be applied to the estimation algorithm.

Fig. 5 shows the maximum crosstalk (V_{max}) with ISI effect, which is predicted by the newly proposed algorithm. Comparing the result of the solution board ($V_{max,s}$) with that of the reference board ($V_{max,r}$), the reduction ratio (R) can be defined as

$$R = \frac{V_{\max,r} - V_{\max,s}}{V_{\max,r}} \times 100\ (\%). \tag{3}$$

The reduction ratio is positive in almost all the bit-rate range except in the range from 0.75 to 0.9 Gbps, which means that the branched reflector can perform well except in this narrow range. However, if we only observe the step response shown in Fig. 4(a), it seems that the reduction ratio will always be about 50%. This indicates that the prediction only based on the step response is not sufficient. In fact, the peak at 0.82 Gbps is primarily caused by the half-wavelength resonance of the slot. Nonetheless, the length of the branched reflector, L_{br}, can slightly affect the resonant frequency. The peak can be moved to lower/higher frequency by increasing/decreasing the value of L_{br}. It is worth noting that the increase/decrease of L_{br} should be kept small because the change will degrade the improvement of V_{max} at other bit rates.

In Fig. 5(a), the frequency response of V_{max} can be divided into three characteristic regions by two frequency points, f_L and f_H. These frequencies can be approximated as

$$f_L = \frac{1}{T_L}, \tag{4}$$

$$f_H = \frac{1}{T_H}. \tag{5}$$

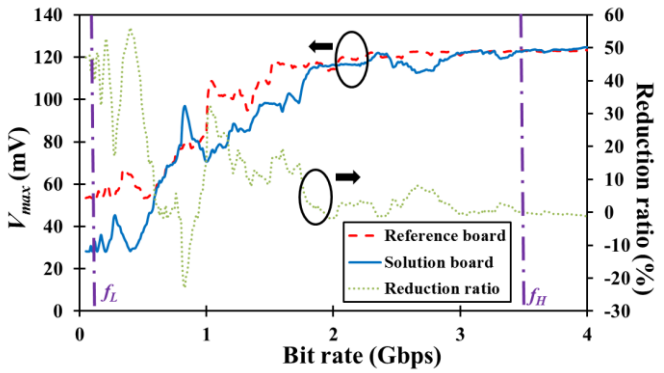
In (4), T_L is defined by the duration time from the peak value of the step response to 5% of its peak value. In this case, the value of T_L is about 10 ns and the resultant f_L is 0.1 Gbps. Meanwhile, T_H in (5) is defined by the time difference between the first transition $V_{1,s}$ ($V_{1,r}$) and the second transition $V_{2,s}$ ($V_{2,r}$) of the step response. In this case, the value of T_H is about 0.28 ns and the resultant f_H is 3.5 Gbps.

The frequency response of V_{max} is almost constant in the two regions below f_L and above f_H, while it varies in the region between f_L and f_H. When the operating speed is below f_L, the ripple of voltage waveform will decay to an insignificant value before the transition of next bit. Therefore, the ISI between the adjacent bits is negligible. Indeed, the value of V_{max} in this range is the same as that of the step response. Fig. 5(b) shows $V_{max,r}$ and $V_{max,s}$, respectively, for the reference and solution boards at the region below f_L. Comparing $V_{max,r}$ ($V_{max,s}$) in this figure with $V_{1,r}$ ($V_{1,s}$) observed from the step response in Fig. 4 (b), good agreement can be seen, which indicates the minor influence of ISI effect.

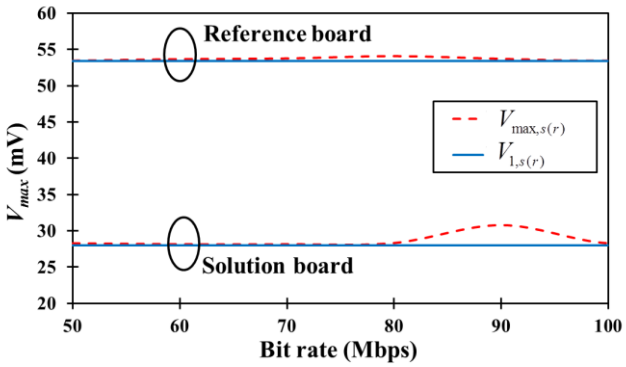
On the other hand, V_{max} is almost frequency-independent and shows the largest value when the bit rate of PRBS is higher than f_H. The reason can be well explained by (1), which is the predicting formula of V_{max}. When the bit rate is fast enough, all the local maxima and minima of the step response will be used to calculate V_{max} in (1). Therefore, the value of V_{max} for small UI (high bit rate) is constant and also is the largest value among all frequency ranges.

B. Experimental Validation

In order to demonstrate the effectiveness of the proposed technique, the solution and reference boards with the same physical dimension as summarized in Table I are fabricated using typical PCB process. Each board has a thickness of 0.8 mm and a relative dielectric constant of 4.4. The experimental results are measured by a time-domain reflectometer (TDR,



(a)



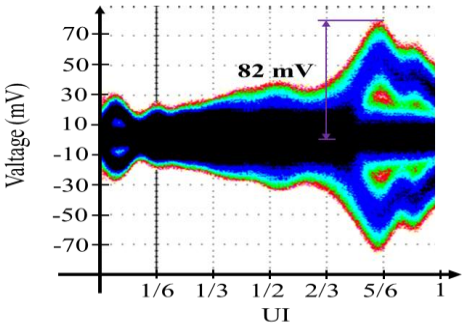
(b)

Fig. 5. Maximum crosstalk with the ISI effect: (a) the entire frequency range, and (b) the enlarged low-frequency region.

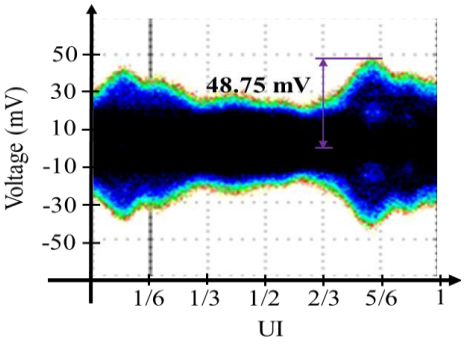
Tektronix CSA 8000B). The PRBS with a magnitude of 0.5 V and a bit rate of 1.2 Gbps generated by a pattern generator (Anritsu MP1763) having a 50-Ω source resistance is fed intothe input end of the microstrip line. All the other ends of the two microstrip lines are terminated by a 50-Ω resistor. The measured results of the near-end crosstalk for the reference and solution boards are illustrated in Figs. 6(a) and 6(b), respectively. Both of them are displayed in the same way with the same data-rate of 1.2 Gbps. As shown in these figures, the maximum near-end crosstalk V_{max} for the solution board is 48.75 mV and that for the reference board is 82 mV, which corresponds to a reduction ratio (R) of about 41%. Meanwhile, the reduction ratio estimated by the proposed algorithm as shown in Fig. 5(a) is about 40%, which is in good agreement with the measurement results.

IV. Conclusion

Since the slot-crossing signal lines are inevitably used in modern package and PCB design, a solution to the slot-induced crosstalk suppression is in urgent need. The branched reflector technique is newly proposed and well demonstrated to suppress the slot-induced crosstalk including the ISI effect. Moreover, the fast prediction algorithm and its flow chart are provided for evaluating the performance of this technique. Through the experiment, the measurement results obtained also show good agreement with the algorithm prediction. Consequently, this new algorithm can be applied to rapidly



(a)



(b)

Fig. 6. Measured near-end crosstalk with the PRBS input: (a) the reference board, and (b) the solution board.

evaluate the ISI-increased slot-induced crosstalk for arbitrary system excitation with any operating speed.

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Circuit/Electromagnetic Hybrid Simulation of Electrostatic Discharge in Contact Discharge Mode

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***Abstract*—In this paper, we describe a hybrid simulation technique for electrostatic discharge (ESD) events in contact discharge mode. The proposed technique is based on circuit, electrostatic field, and full-wave simulations. Because the hybrid simulation can take a low computational cost relative to existing full-wave techniques, it can reduce the total CPU time and the amount of memory consumption.**

I. Introduction

Electrostatic discharge (ESD) causes failures and damage to electronic equipments because the current produced by a human-to-metal (HTM) discharge has high-frequency components due to the fast rise time of the current waveform. In order to ensure immunity-aware electromagnetic compatibility (EMC) design, it is necessary to simulate the actual ESD events along the IEC 61000-4-2 [1]. Although some papers describe about the numerical modeling and simulation techniques for the ESD [2]–[5], it is still one of challenging issues in the EMC community to deal with the physical phenomena of the discharge and include them for the numerical simulation.

The three-dimensional electromagnetic simulation provides full-wave solutions as spatially-distributed field components generated by discharging [4]–[7]. However, the computational cost, the CPU time and memory requirement of the electromagnetic analysis tend to be large compared to the circuit-based simulation. On the other hand, some circuit models of ESD generators have been developed [5] and [8]. Since the circuit model includes the elements which represent only major effects during the discharging process, its computational cost is much lower than that of the full-wave simulation.

In this paper, we describe a hybrid technique combining the circuit and full-wave simulations for the ESD events in the contact discharge mode. The proposed technique receives benefits of the low computational cost of the circuit simulation and, at the same time, can obtain the electromagnetic field distribution from the full-wave simulation.

II. Existing FDTD Solver for the ESD Events

The existing full-wave simulation techniques applied to the immunity test use either a commercially-based full-wave simulator or an FDTD solver [4]–[7]. In this paper, we follow the FDTD simulation proposed in [6] with some modifications. In [6], a Noiseken ESD generator and a test setup according to the IEC standard are modeled in a computational domain. The domain is discretized into the Yee grid, and the whole domain to be simulated is shown in Fig. 1(a). In addition, the detailed structure of the ESD generator is also illustrated in Fig. 1(b). The ESD generator includes the capacitor unit, resistor, and electrode. The capacitor unit and electrode are aluminium and the resistor has the conductivity of 2.41 S/m. In addition to the actual objects, we insert some lumped elements into three parts, namely, charging, switching, and target parts as shown in Fig. 1(b). Furthermore, free space surrounding the domain is truncated by the absorbing boundary which is placed at the area immediately external to the domain.

The transient simulation performed in [6] is separated into two phases, namely, charging and discharging phases. In both the phases, a time-dependent voltage source V_c is inserted into the charging part, and its value is defined as

$$V_c(t) = \begin{cases} V_0\left(1-e^{\frac{-t}{\tau}}\right) & (0 \le t \le \tau_0) \\ V_0\left(1-e^{\frac{-\tau_0}{\tau}}\right) - \dfrac{1}{C_s}\displaystyle\int_{\tau_0}^{t} i_c(\xi)d\xi & (\tau_0 < t) \end{cases}, \quad (1)$$

where τ is the time constant of charging, τ_0 is the stop time of charging, V_0 is the high voltage supply, C_s is the value of the storage capacitor, and i_c is the current flowing through V_c. In fact, the first equation in (1) is used for the charging process, and the second one relates to the discharging process. Additionally, the target, into which the current is injected, is modeled as the load resistor R_L and inserted into the target part shown in Fig. 1(b). As for the switching part, the capacitor C_{sw} is used in both the phases whereas the inductor L_{sw} is inserted only in the discharging phase. In the simulations performed in Section IV, we set the parameters so that $\tau = 30$ ns, $\tau_0 = 5\tau$, $V_0 = 5$ kV, $C_{sw} = 0.8$ pF, $L_{sw} = 70$ nH, and $R_L = 2\ \Omega$.

III. Hybrid Simulation for the ESD Events

The proposed technique is separated into three processes, and their outlines are as follows:

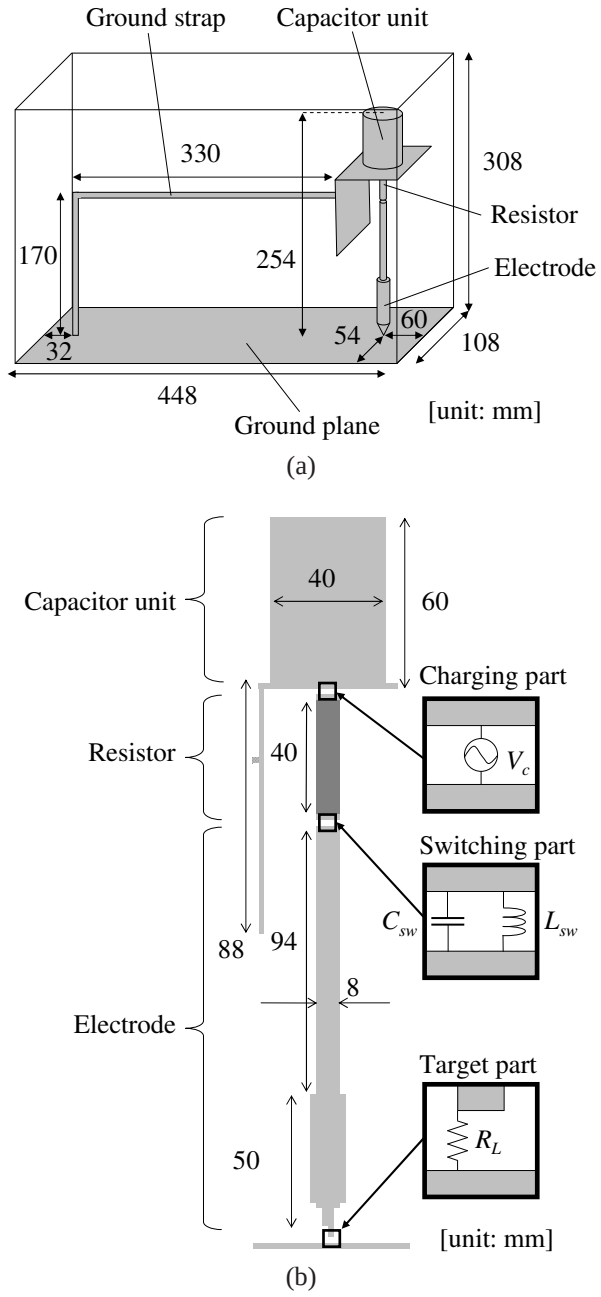

Fig. 1. The dimensions and structures of the computational domain including the ESD generator, ground strap, target, and large metal plate. The absorbing boundary exists around the domain. (a) The dimensions of the whole system. (b) The detailed dimension and structure of the ESD generator.

1) *The estimation of input currents*: we perform the transient simulation of the equivalent circuit model of an ESD generator to obtain the current injected into a target and one flowing through a ground strap. These currents are used as inputs for the discharging phase.
2) *The calculation of initial electric field distribution*: given voltages on the conductors of a storage capacitor, potentials distributed over a computational domain are calculated by solving the Laplace's equation. The initial values of the electric fields used in the next process are calculated from the potentials.
3) *Full-wave simulation for the discharging phase*: the electromagnetic fields generated by the discharge current flowing through the target are calculated using the FDTD-based modeling and simulation.

In fact, the first and second processes are preparation for the third process, and therefore, we do not care the order of the first two processes. The above three processes are described in detail below.

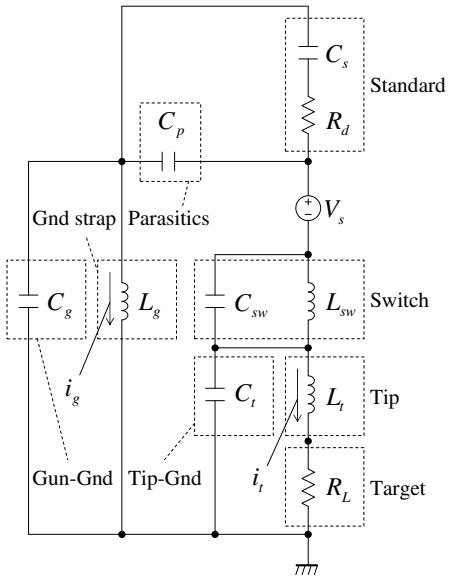

Fig. 2. The proposed equivalent circuit model of the ESD generator.

TABLE I
PARAMETERS IN THE CIRCUIT MODEL

Category	Element type	Parameter	Value
Standard	Storage cap. (pF)	C_s	150
	Discharge res. (Ω)	R_d	330
Parasitics	Cap. (pF)	C_p	0.9
Switch	Cap. (pF)	C_{sw}	0.8
	Ind. (nH)	L_{sw}	70
Tip	Ind. (nH)	L_t	11
Tip-Gnd	Cap. (pF)	C_t	7.3
Gun-Gnd	Cap. (pF)	C_g	4.3
Gnd strap	Ind. (nH)	L_g	600
Target	Res. (Ω)	R_L	2
Excitation	Voltage source	V_s	–

A. Circuit Simulation for the Estimation of the Input Currents

The conventional circuit models of the ESD generator in [4], [5], [8], [9] mainly include a storage capacitor $C_s = 150$ pF and a discharge resister $R_d = 330\ \Omega$ according to the IEC standard. Although the values of circuit parameters vary depending on a product type of an ESD generator, the existing

models deal with some common components; the material of the generator; parasitic coupling; ground strap; and target objects. Especially, because the return path of the discharge current and the parasitic elements directly affect the waveform of the discharge current, we have to include them in the equivalent circuit model.

We synthesized the circuit model of the ESD generator in the previous section and it is illustrated in Fig. 2. And the related circuit parameters are shown in Table I. The circuit is composed of the elements associated with the RC circuit used in the IEC standard, parasitic elements, materials of the generator body, discharge tip, and return path. In this synthesis, the return path is represented by two elements. The first one is the capacitor C_g, which affects the current value and the rising time before the first peak. The other is the inductor L_g, which corresponds to the ground strap and affects the current value and the appearance time of the second peak. To perform the transient simulation by using a SPICE-like simulator, it is assumed that the network is driven by the independent voltage source V_s which is given by a step function. This means that the real discharging process of the charge is replaced by the charging process of the storage capacitor [9].

The currents are calcurated by the transient simulation of Fig. 2. We can obtain the current i_t flowing through the tip inductor L_t and the current i_g flowing through the ground strap inductor L_g specified in Fig. 2. We use these currents as the inputs for the full-wave simulation in the proposed method.

B. Electrostatic Field Simulation for the Calculation of Initial Electric Field Distribution

After the ESD generator is charged, it is expected that an electric field is generated around the generator due to the charge distributed over the conductor surfaces of the storage capacitor. Therefore, we need to know electric field distribution before starting the transient simulation for the discharging phase. In order to obtain the distribution after charging, we begin with the Laplace's equation in three-dimensional space

$$\frac{\partial^2\phi(x,y,z)}{\partial x^2}+\frac{\partial^2\phi(x,y,z)}{\partial y^2}+\frac{\partial^2\phi(x,y,z)}{\partial z^2}=0, \qquad (2)$$

where ϕ is the scalar potential. In this paper, we solve (2) numerically by means of the finite difference method (FDM) [10]. Then, we get a set of simultaneous equations. To solve the simultaneous equations, we adopt a conventional iterative solver, the successive over relaxation (SOR) method [11]. The grid used in the FDM is compatible with the Yee grid used in the FDTD method in the discharge phase.

C. Full-Wave Simulation for the Discharging Phase

In the third process, the full-wave simulation is performed using those pre-calculated values. Actually, we adopt the FDTD method and simulate the reduced computational domain shown in Fig. 3 instead of the domain defined in Fig. 1(a). The reduced domain is derived by removing the upper part of Fig. 1(a). Before starting the transient simulation, we set the initial values of the electric field obtained from the electrostatic field simulation in the second process. Then, the transient responses are calculated step by step along the time marching procedure of the FDTD method. In this case, excitations are exactly the same as the currents i_t and i_g obtained from the circuit simulation in the first process. These currents are inserted as independent current sources as illustrated in Fig. 3. Clearly, because the computational domain in our method is smaller than that of the existing FDTD solver, it is expected that the proposed method can reduce the computational cost significantly.

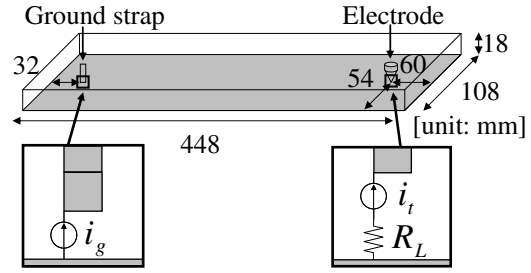

Fig. 3. The dimensions and structures of the reduced computational domain used for the full-wave simulation of the proposed technique.

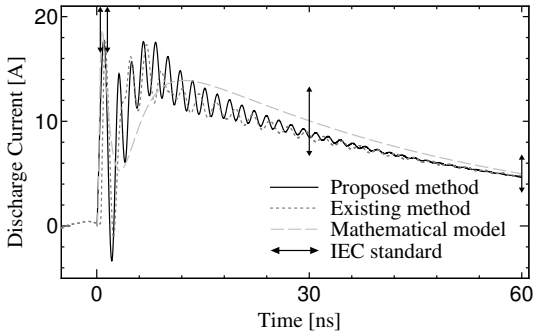

Fig. 4. The waveform results of the discharge current flowing through the target.

IV. Numerical Results and Discussion

We perform transient simulations using the existing FDTD solver and the proposed hybrid technique. In the FDTD-based simulation of both the proposed and existing methods, the objects and space to be analyzed are discretized using a cubic cell of 2 mm on a side. We also use a perfectly matched layer (PML) which is 16 cells thick as the absorbing boundary to truncate the computational domain.

The waveform results of the discharge currents are shown in Fig. 4(a). For comparison, a waveform calculated by a mathematical model described in [4] is also plotted as a reference one in these figures. Each of the values from the proposed method is nealy equal to that from the existing one, and all the values are within the tolerance defined in the IEC standard. From the above results, it is confirmed that the waveform of the discharge current obtained by the proposed method is as accurate as the one by the existing full-wave

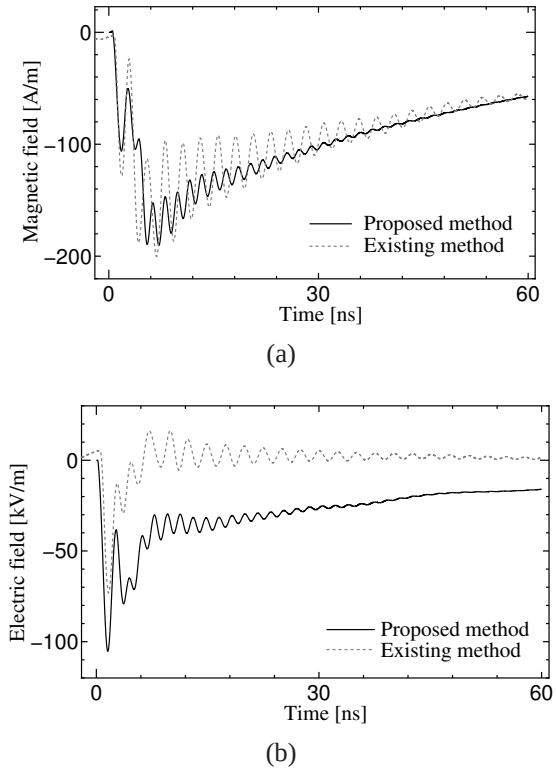

Fig. 5. The waveform results of field intensities. (a) Magnetic field intensity. (b) Electric field intensity.

solver.

The electromagnetic fields are also calculated and we observe those at the obsevation points which are placed at the distance of 50 mm from the discharge point. The observed electric field and magnetic field intensities are illustrated in Fig. 5. From Fig. 5(a), it is confirmed that the waveform of the magnetic field intensity from the proposed method is approximately similar to that from the existing method. In contrast, there is a difference between the electric field intensities shown in Fig. 5(b) after the first peak. We presume that one of the reasons for the difference between the electric field intensities is because the current path in our computational domain does not include the ground strap, and thereby we ignore the electromagnetic effect from the ground strap in the reduced domain.

From the numerical result, the proposed method can reduce the whole computational time and is totally about 4.4 times faster than the existing solver. The amount of the memory used during the simulation of our solver is 515 296 KB and that of the existing one is 1 758 832 KB. This means that the proposed method can reduce the required memory capacity by 70 %.

V. Conclusions and Future Works

We have proposed the hybrid simulation technique for the simulation of the ESD events in the contact discharge mode. The proposed method was described separately divided into the three processes. From the numerical results, we have confirmed that our technique can perform about 4.4 times faster simulation than the existing FDTD solver.

Although the proposed method is more efficient and can produce the adequate waveform of the discharge current, the accuracy of the field components is not good enough. The difference between the results from the existing and the hybrid solvers is caused by the simple hybridation in the proposed technique. Therefore, we have to improve the ways to separate the system to be analyzed into subdomains and combine the results obtained from the separated subdomains. This consideration is necessary for the hybrid simulation to provide more accurate results of electromagnetic field distribution generated by the ESD events.

Acknowledgement

We would like to express the special thanks to SESAME Technology Inc. for the technical advice.

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Output Signal Synthesis of Nonlinear Digital Channel Using Superposition of Multiple Edge Responses

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I. INTRODUCTION

The pseudo-random bit sequence (PRBS) simulation takes more and more time due to the increasing circuit complexity. Several methods using superposition technique have then been proposed to obtain the output waveform quickly. These methods began with expressing an arbitrary input data $b[n]$ as a linear combination of elementary functions (e.g., unit step) as:

$$\begin{aligned} x(t) &= \sum_{n=0}^{\infty} (b[n]-b[n-1])\ u(t-nUI) \\ &= \sum_{n=0}^{\infty} b[n]\ (u(t-nUI)-u(t-(n-1)UI)), \end{aligned} \quad (1)$$

where $x(t)$ is the input waveform, UI the unit interval, and $u(t)$ the unit step function, assuming $b[n]=0$ for $n<0$. The next step is to analytically express the output as a function of $b[n]$. Casper et al. [2], starting from the second line of (1), built the output using single bit response (SBR), or '010' response, as

$$y(t) = \sum_{n=0}^{\infty} b[n]\ \varphi(t-nUI), \quad (2)$$

where $y(t)$ is the output waveform and $\varphi(t)$ the SBR. Shi et al. [3], starting from the first line of (1), constructed the output waveform using one rising transition response, or '01' response, and one falling transition response, or '10' response, as

$$y(t) = \sum_{n=0}^{\infty} |b[n]-b[n-1]|\, s^{b[n]}(t-nUI), \quad (3)$$

where $s^{b[n]}$ is the '01' or '10' response if $b[n]=1$ or 0. Ren et al. [1] constructed the output waveform using multiple edge responses (MER) as

$$y(t) = \sum_{n=0}^{\infty} |b[n]-b[n-1]|\ S^{b[n-m]..b[n-1]}(t-nUI), \quad (4)$$

where $S(t)$ is the particular rising or falling edge response when the m preceding bits are $b[n\text{-}m]$ to $b[n\text{-}1]$. We term m the order of the method. From (2~4), we can see the superposition principle: the output signal can be constructed using only a few simple responses.

Limitation exists, though. A completely linear system is assumed by (2), and (3) as well except that the '01' and '10' responses are allowed to be different. Only (4), theoretically, is promised to work for arbitrary nonlinear system, as long as the order m is chosen high enough.

II. BRIEF INTRODUCTION TO THE ALGORITHM

A. Superposition of Multiple Edge Response

Definition: An edge response is defined as the output response when the input undergoes a '01' or '10' transition with some particular preceding bit pattern. For a linear system, the '10' response is exactly the inverse of the '01' response, and all '01' or '10' responses are always the same no matter what happened previously. For a nonlinear system, neither of the above properties is true. For example, the '01' responses (the underlined portions) to the input '0<u>01</u>' and '1<u>01</u>' are in fact different because a '10' transition just before the target '01' transition in the second input will alter the system greatly, e.g. by causing a voltage ripples in the PDN, as illustrated in Fig. 1. For such systems, errors occur if one uses (2) or (3) to build the output. The MER method cleverly solves this problem by using more than two edge responses to build the output. Thus, the nonlinear effects such as the voltage ripples in PDN due to earlier transitions can be stored in these edge responses.

Example: one can choose to use 4 edge responses, as defined in Table I, to construct the output waveform. In this table, $y^{abc}(t)$ denotes the output signal to the input bit pattern 'abc'. These 4 responses together correspond to a 2^{nd}-order MER since all possible input bit patterns, up to 2 bits before the target '01' or '10' transition, i.e., the last transition, are considered. As an example, to construct the output due to input '00101101' using 2^{nd} order MER, according to (4), we have

$$y(t)=r^{001}(t)+f^{010}(t-UI)+r^{101}(t-2UI)+f^{110}(t-4UI)+r^{101}(t-5UI).$$

In general, an m'th order MER stores a total of 2^m edge responses. Edge responses up to order 5 are listed in Table II, where $r^{abc01}(t) = y^{abc01}(t) - y^{abc00}(t)$.

The reason that the MER method can include nonlinear effects is that: Nonlinearity decays to zero in the end. For example, voltage ripples on the PDN due to earlier transitions cannot last forever. The PDN voltage will saturate in the end. It can be expected that rising transitions $r^{101}(t)$ and $r^{001}(t)$ are different, but $r^{10000001}(t)$ and $r^{001}(t)$ shall be quite similar. Thus by storing enough amounts of edge responses, nonlinear effects can be well captured. This is the basic idea of MER.

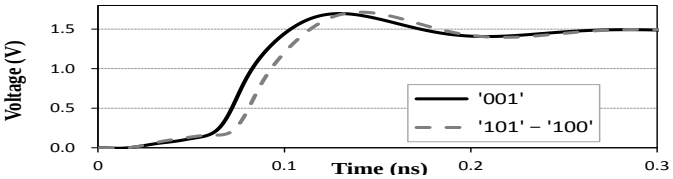

Figure 1. Different '01' transitions.

TABLE I. DEFINITION OF 2ND ORDER BP RESPONSES

Name	Definition	Name	Definition
$r^{001}(t)$	$y^{001}(t)$	$f^{110}(t)$	$y^{110}(t)$
$r^{101}(t)$	$y^{101}(t) - y^{100}(t)$	$f^{010}(t)$	$y^{010}(t) - y^{011}(t)$

TABLE II. BP RESPONSES UP TO 5TH ORDER

Order	Rising Transitions [a]	Falling Transitions
1	r^{01}	f^{10}
2	r^{101}	f^{010}
3	r^{1001}, r^{0101}	f^{0110}, f^{1010}
4	$r^{10001}, r^{01001}, r^{01101}, r^{10101}$	$f^{01110}, f^{10110}, f^{10010}, f^{01010}$
5	$r^{100001}, r^{010001}, r^{011001}, r^{101001}$ $r^{011101}, r^{101101}, r^{100101}, r^{010101}$	$f^{011110}, f^{101110}, f^{100110}, f^{010110}$ $f^{100010}, f^{010010}, f^{011010}, f^{101010}$

a. All '(t)'s are omitted for simplicity.

III. TEST RESULTS

A. Test Circuit

The test circuit is a 4-stage CMOS inverter with power /ground nets connected to PDN before to the ideal power /ground as shown in Fig. 2. The PDN is an RLC T model and the values are typical of a package level PDN (see, for example, [4]). Board level PDN is omitted deliberately to make the PDN worse. The input data rate is 10 Gb/s with rise/fall time 10 ps.

B. Difference between Edge Responses

The edge responses r^{01}, r^{101}, r^{0101}, and r^{10101} shown in Fig. 3 illustrate that the differences between subsequent waveforms become smaller when the order increases, which follows the basic idea of MER. A quantitative comparison for rising transitions up to order 5 is listed in Table III, where the difference $DR_{xxx,yyy}$ is defined as the absolute area between rising transitions r^{xxx}, and r^{yyy} as

$$DR_{xxx,\,yyy} = \int \left| r^{xxx} - r^{yyy} \right| dt. \qquad (5)$$

Table III is organized in a manner that each row itself makes up a comparable series. For example, in the first row, $DR_{01,101}$ =24.5 quantifies the impact of the '10' transition 1 bit earlier, and $DR_{101,0101}$ = 8.7 indicates that the influence of the '01' transition 2 bits earlier is smaller. $DR_{0101,10101}$ and $DR_{10101,010101}$ are even smaller, which conforms to the basic idea of MER. Most of the rows follow this trend.

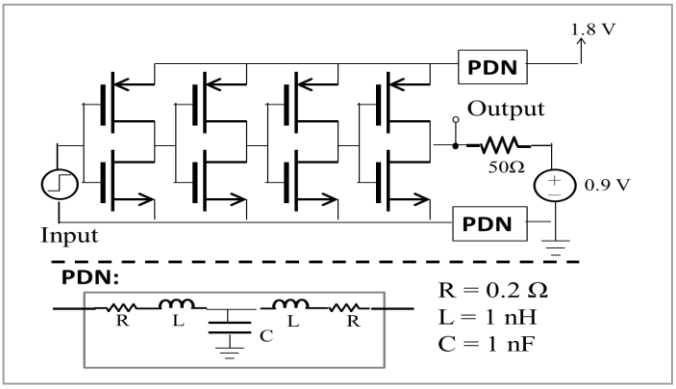

Figure 2. The test circuit consists of 4 CMOS inverters as an output driver and 2 T-model RLC power distribution networks.

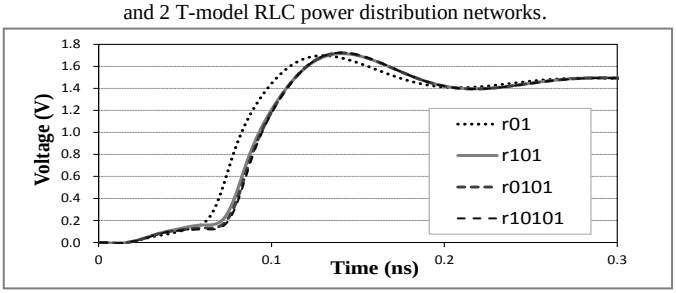

Figure 3. Four BP responses of the test circuit. The difference between subsequent waveforms decreases when the order increases.

TABLE III. COMPARISON OF RISING TRANSITIONS

$DR_{01,101}$= 24.5[a]	$DR_{101,0101}$=8.7	$DR_{0101,10101}$=6.2	$DR_{10101,010101}$=6.0
		$DR_{0101,100101}$=4.8	
	$DR_{101,01101}$=5.8	$DR_{01101,101101}$=5.4	
	$DR_{101,011101}$=5.6		
$DR_{01,1001}$=10.1	$DR_{1001,01001}$=8.0	$DR_{01001,101001}$=5.7	
	$DR_{1001,011001}$=5.1		
$DR_{01,10001}$=5.0	$DR_{10001,010001}$=6.3		
$DR_{01,100001}$=4.6			

a. The units are all ps×V.

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Macromodeling and Circuit Simulation of High-Speed Interconnects Based on Vector Fitting and Equivalent Circuit Synthesis

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Abstract

This paper describes a way to approximate the frequency response of interconnects by using a rational function and synthesize a SPICE-compatible equivalent circuit from the function. We introduce the vector fitting (VF) to derive the rational function in the pole-residue form from the dataset of the frequency response. Then, the state equation which has only a real number is realized using the Jordan canonical form and proper similarity transformation. The SPICE-compatible circuit is synthesized from the state equation with dependent sources in addition to RC lumped elements. We provide the numerical results for an example system which represents a simplified transmission line and discuss about the availability of the VF and equivalent circuit realization technique.

1. Introduction

One of the problems in the recent advanced integration technologies is that the space to which electronic circuits are mounted is limited to a small area. In this situation, interferences among them become significant, especially, those inside mobile and in-vehicle electronic devices. Therefore, it becomes a challenging issue to ensure signal integrity (SI) of the electronic circuits because of the signal delay, reflection, skin effect, and cross talk caused by the high-frequency components of the signal [1]. In order to lead SI-aware design, it is necessary to consider not only the electrical behavior of the circuit but also the electromagnetic characteristics of surrounding components. For this purpose, it becomes more and more important to develop the modeling and simulation techniques for high-speed interconnects in the next-generation circuit design [2, 3].

In general, the characteristics of the high-speed interconnects can be represented by frequency responses, such as the Z, Y, and S-parameters, which tend to be provided in the form of discrete data from measurements or full-wave simulations. In particular, in the case that we deal with electronic components interconnected with each other, the S parameters are widely used because they are useful to represent the relations among systems from a viewpoint of the characteristic impedance.

In This paper, we describe a way to include the discrete data of the frequency response to circuit simulations [4–6]. The way that we introduce consists of three procedures: a rational function approximation of the frequency response; state-space realization; and a SPICE-compatible equivalent circuit synthesis.

The remainder part of the paper is organized as follows. In Section II, we introduce the vector fitting (VF) to derive the rational function approximation of the frequency response. Then, in Section III, the state equation is derived from the rational function. Subsequently, The equivalent circuit associated with the state equation is obtained in Section IV. The availability of the above techniques is demonstrated by showing some numerical results in Section V. Finally, we conclude the paper in Section VI.

2. Rational Approximation Using Vector Fitting (VF)

We adopt VF to derive the rational function in the pole-residue form from the dataset of the frequency response because the function obtained by VF is accurate and always stable [7, 8]. In VF, it is assumed that a frequency response function $F(s)$ is approximated as the rational function in the pole-residue form

$$F(s) \approx \sum_{n=1}^{N} \frac{r_n}{s - p_n} + d \tag{1}$$

where N is the order of the rational function, $s = j\omega$, j is the imaginary unit, ω is the angular frequency, and d is the real constant while the poles p_n and residues r_n are either real or complex conjugate pairs. The VF algorithm separates the calculations of the poles, residues, and d in (1) into two processes: the poles are obtained in the first process, and the

residues and d are calculated in the second one. To identify the poles, we first define an unknown weighting function $\sigma(s)$ and a weighted function $\sigma(s)F(s)$ as rational functions as follows:

$$\sigma(s) = \sum_{n=1}^{N} \frac{\tilde{r}_n}{s-\tilde{p}_n} + 1 \tag{2}$$

$$\sigma(s)F(s) = \sum_{n=1}^{N} \frac{r_n}{s-\tilde{p}_n} + d \tag{3}$$

where $\tilde{p}_n$ and $\tilde{r}_n$ are the poles and residues of $\sigma(s)$. Note that the poles of the weighted function are the same as those of $\sigma(s)$, and its residues are the same as those in (1). Substituting (2) into (3) and rearranging the equation lead to

$$\sum_{n=1}^{N} \frac{r_n}{s-\tilde{p}_n} + d - \left(\sum_{n=1}^{N} \frac{\tilde{r}_n}{s-\tilde{p}_n} \right) F(s) = F(s). \tag{4}$$

Given $\tilde{p}_n$ as known initial poles and $F(s)$ at K frequency points, we get K linear equations in the form of (4). Assembling those equations leads to the overdetermined linear problem

$$\mathbf{\Phi z} = \mathbf{f} \tag{5}$$

where $\mathbf{\Phi}$ is $K \times (2N+1)$ matrix, $\mathbf{z}$ is the unknown vector of which the size is $2N+1$, and $\mathbf{f}$ is the vector of which the size is K. Since the unknown vector is composed of r_n, d, and $\tilde{r}_n$, we can obtain $\tilde{r}_n$ by solving (5). In fact, the poles p_n of (1) are equal to the zeros of $\sigma(s)$, and these zeros can be found by calculating the eigenvalues of a matrix

$$\mathbf{Q} = \hat{\mathbf{A}} - \hat{\mathbf{b}}\hat{\mathbf{c}} \tag{6}$$

where $\hat{\mathbf{A}}$ is the diagonal matrix of which the elements are $\tilde{p}_n$, $\hat{\mathbf{b}}$ is the column vector of ones, and $\hat{\mathbf{c}}$ is the row vector containing $\tilde{r}_n$. The eigenvalues of (6) provide a new set of poles, and the new poles are used as $\tilde{p}_n$ in (4) to construct the overdetermined problem (5) again. By iterating solving (5) and calculating the eigenvalues of (6), the new set of poles converges to p_n. Once p_n is obtained, the accurate values of the residues r_n and d can be calculated by solving the other overdetermined problem, which is derived from (1) in a similar manner to the way to derive (5) from (4).

3. State-Space Realization

The rational function (1) obtained by VF can be rewritten in detail as follows:

$$F(s) = \sum_{n=1}^{N_r} \frac{r_{r,n}}{s-p_{r,n}} + \sum_{n=1}^{N_c} \left(\frac{r_{c,n}}{s-p_{c,n}} + \frac{r_{c,n}^*}{s-p_{c,n}^*} \right) + d \tag{7}$$

where p_r and r_r are the real poles and residues, p_c and r_c are the complex poles and residues, $*$ denotes the complex conjugate, N_r is the number of the real poles, N_c is the number of the complex conjugate pairs, and $N = N_r + 2N_c$. Assuming each element of the transfer function matrix

$$\mathbf{H}(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D} \tag{8}$$

has the form of (7), the associated state equation which has M state variables and P ports can be written as follows:

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{Ax} + \mathbf{Bu} \\ \mathbf{y} = \mathbf{Cx} + \mathbf{Du} \end{cases} \tag{9}$$

where $\mathbf{x}$ is the state variable vector, $\mathbf{u}$ and $\mathbf{y}$ are the input and output vectors, $\mathbf{A}$ is $M \times M$ diagonal matrix containing the poles, $\mathbf{B}$ is $M \times P$ matrix containing 0 or 1, $\mathbf{C}$ is $P \times M$ matrix containing the residues, $\mathbf{D}$ is $P \times P$ matrix containing the real constants. More specifically, (9) is written as the Jordan canonical form

$$\begin{cases} \begin{bmatrix} \dot{\mathbf{x}}_r \\ \dot{\mathbf{x}}_{c,1} \\ \dot{\mathbf{x}}_{c,2} \end{bmatrix} = \begin{bmatrix} \mathbf{A}_r & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_c & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{A}_c^* \end{bmatrix} \begin{bmatrix} \mathbf{x}_r \\ \mathbf{x}_{c,1} \\ \mathbf{x}_{c,2} \end{bmatrix} + \begin{bmatrix} \mathbf{B}_r \\ \mathbf{B}_c \\ \mathbf{B}_c^* \end{bmatrix} \mathbf{u} \\ \mathbf{y} = \begin{bmatrix} \mathbf{C}_r & \mathbf{C}_c & \mathbf{C}_c^* \end{bmatrix} \begin{bmatrix} \mathbf{x}_r \\ \mathbf{x}_{c,1} \\ \mathbf{x}_{c,2} \end{bmatrix} + \mathbf{Du} \end{cases} \tag{10}$$

where the submatrices and vectors with the subscript r are related to the real number, and those with the subscript c are related to the complex number. In order to make (10) have only real numbers, we perform a similarity transformation. The transformation is introduced by replacing $\mathbf{x}$ by $\mathbf{J}^{-1}\tilde{\mathbf{x}}$ and premultiplying $\mathbf{J}$ by the first equation of (10), where $\mathbf{J}$ is a transformation matrix

$$\mathbf{J} = \begin{bmatrix} \mathbf{I} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{I} & \mathbf{I} \\ \mathbf{0} & j\mathbf{I} & -j\mathbf{I} \end{bmatrix} \tag{11}$$

and $\mathbf{I}$ is the unit matrix. As a result, we get the real state equation composed only of real numbers

$$\begin{cases} \begin{bmatrix} \dot{\tilde{\mathbf{x}}}_r \\ \dot{\tilde{\mathbf{x}}}_{c,1} \\ \dot{\tilde{\mathbf{x}}}_{c,2} \end{bmatrix} = \begin{bmatrix} \mathbf{A}_r & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathrm{Re}(\mathbf{A}_c) & \mathrm{Im}(\mathbf{A}_c) \\ \mathbf{0} & -\mathrm{Re}(\mathbf{A}_c) & \mathrm{Re}(\mathbf{A}_c) \end{bmatrix} \begin{bmatrix} \tilde{\mathbf{x}}_r \\ \tilde{\mathbf{x}}_{c,1} \\ \tilde{\mathbf{x}}_{c,2} \end{bmatrix} + \begin{bmatrix} \mathbf{B}_r \\ 2\mathrm{Re}(\mathbf{B}_c) \\ -2\mathrm{Im}(\mathbf{B}_c) \end{bmatrix} \mathbf{u} \\ \mathbf{y} = \begin{bmatrix} \mathbf{C}_r & \mathrm{Re}(\mathbf{C}_c) & \mathrm{Im}(\mathbf{C}_c) \end{bmatrix} \begin{bmatrix} \tilde{\mathbf{x}}_r \\ \tilde{\mathbf{x}}_{c,1} \\ \tilde{\mathbf{x}}_{c,2} \end{bmatrix} + \mathbf{Du} \end{cases} \tag{12}$$

where $\tilde{\mathbf{x}} = [\tilde{\mathbf{x}}_r^{\mathrm{T}} \ \tilde{\mathbf{x}}_{c,1}^{\mathrm{T}} \ \tilde{\mathbf{x}}_{c,2}^{\mathrm{T}}]^{\mathrm{T}}$.

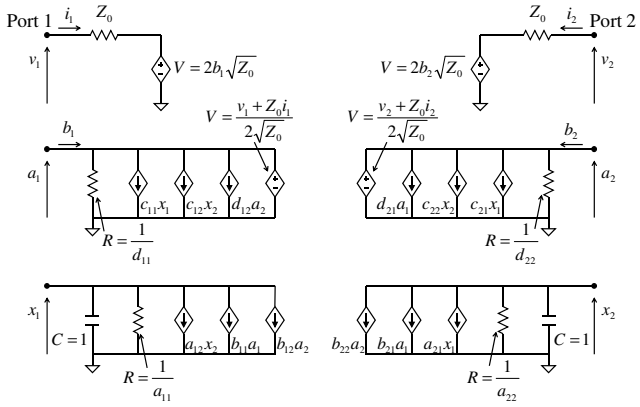

Fig. 1: The equivalent circuit realization of the S-parameters

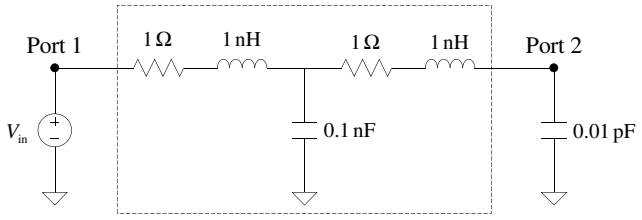

Fig. 2: The example circuit

4. Equivalent Circuit Synthesis

It has been reported that the circuit synthesized using only passive RLC elements may be nonpassive because the values of the elements may become negative [9, 10]. Therefore, we adopt another technique, which uses control sources in addition to RC elements and can always synthesize the network that is able to be analyzed by using SPICE-like simulators [4, 11]. To illustrate this technique, we use the simple state equation of which the transfer function represents the S-parameter. The example system has two ports and two state variables as

$$\begin{cases} \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \\ \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} d_{11} & d_{12} \\ d_{21} & d_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \end{cases} \tag{13}$$

where a_p and b_p are the incident and reflected waves at the port p, and they are related to the port voltage v_p and current i_p as

$$a_p = \frac{v_p + Z_0 i_p}{2\sqrt{Z_0}}, \quad b_p = \frac{v_p - Z_0 i_p}{2\sqrt{Z_0}} \tag{14}$$

where Z_0 is the reference impedance. In order to solve the ordinary differential equations (ODEs) (13) along with (14) by using the SPICE-like simulator, we assume that each ODE in (13) fulfills Kirchhoff's current law (KCL), and the equations in (14) are derived from Kirchhoff's voltage law (KVL). This can be achieved by regarding the state variable and a_p as the voltages, the coefficient related to the state variable as resistance or the transconductance of a voltage control current source (VCCS), and the coefficient related to the derivative of the state variable as capacitance. For instance, by assuming the first equation of (13) is the KCL equation related to the node with the voltage x_1, we can synthesize the circuit in which the capacitor of 1 F, resistor of $1/a_{11}$ Ω, and VCCSs, of which the transconductances are a_{12}, b_{11}, and b_{12}, respectively, are connected in parallel to each other. Fig. 1 shows the schematic of the circuit associated with (13) and (14). In a similar manner, we can apply the above synthesis technique to arbitrary state space equations.

5. Numerical Results

As an example application of the above approaches, we deal with the circuit illustrated in Fig. 2. In Fig. 2, the part surrounded by the dotted line represents the equivalent circuit model of a simple transmission line. We regard this part as the two-port network to which the voltage source V_{in} is connected at Port 1 and the capacitor of 0.01 pF is connected at Port 2. The values of the other elements are shown in Fig. 2.

First, the S-parameters of the two-port network and their rational approximation obtained by VF are plotted in Fig. 3. In this case, we provide three rational functions of which the orders N are 2, 3, and 6, respectively. As shown in Fig. 3, the S-parameters calculated from the functions of which the orders are 3 and 6 completely agree with the analytical solution in the given frequency range while the results from the lower order function is slightly different from the others.

Next, we perform the transient simulations using LTspice for the original circuit in Fig. 2 and the equivalent circuits synthesized from the rational functions. For this purpose, the waveform of V_{in} is set to the trapezoidal pulse of which the rise and fall times are 0.5 ns and the pulse width is 10 ns. The transient responses observed at Port 2 are plotted in Fig. 4. As we can see in Fig. 4, the waveform from the function with $N = 3$ agrees well with one from the original circuit. In contrast, the transient response from the function with $N = 6$ does not completely agree with one from the original circuit though the rational function is accurate in the frequency domain. This may be because the higher order function has an error at the high frequency range which does not shown in Fig. 3. The waveform from the lower order function also does not agree with the original one as we expected.

6. Conclusion

In this paper, we have introduce one of the ways to include

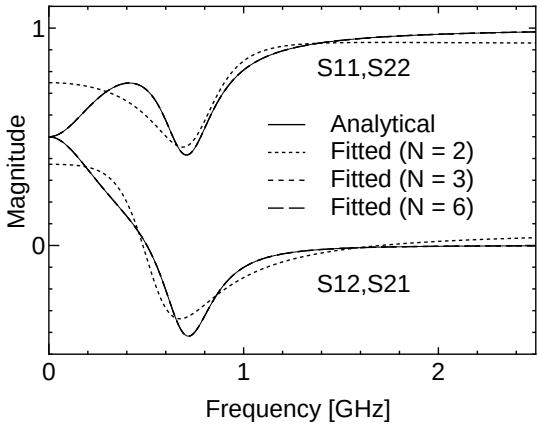

Fig. 3: The S-parameters of the two-port network in Fig. 2

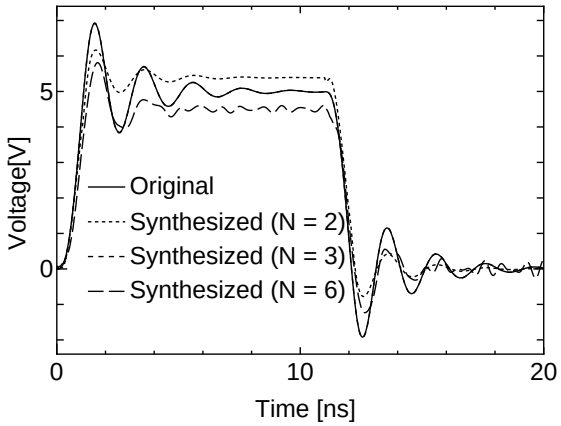

Fig. 4: The transient response at Port 2

the discrete data of the frequency response to the circuit simulation. The VF algorithm was adopted to derive the rational function approximation in the pole-residue form, and the SPICE-compatible equivalent circuit was obtained from the state equation associated with the rational function. From the numerical results, it has been confirmed that the S-parameters of the simple transmission line can be approximated accurately by using VF. Moreover, the equivalent circuit derived using the circuit synthesis technique could be applied to the transient simulation performed by the conventional SPICE-based simulator. We saw that the order of the rational function should not be too low or too high in order to produce the accurate results in the time domain.

Acknowledgment

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A Compact and Broadband Forward-Wave Directional Coupler with Arbitrary Coupling Levels

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***Abstract* — A novel broadband and compact forward-wave directional coupler is proposed. The broadband impedance matching of the even- and odd-mode of the proposed coupler can be achieved, and the phase difference between the even- and odd-mode can keep approximately at a constant level during a broad frequency range. The equivalent models are constructed to predict the propagation properties based on the Bloch-Floquet theorem. This three-layer structure is fabricated on the Duroid substrate. The coupling level is -3.8 ± 0.5 dB from 1.97 GHz to 2.85 GHz and the corresponding fractional bandwidth is 37%. Besides, the size is only 0.4 λg. Compared to the previous works, the proposed structure can be designed with wider operational bandwidth and a smaller size.**

***Index Terms* – forward-wave directional coupler. broadband.**

I. Introduction

Forward-wave directional coupler (FWDC) is an important component in communication system and is often used for power dividing and power combining. It is often applied in the circuit design for performance enhancement, such as filter, amplifiers, mixers, and modulators [1]. The coupling level of the forward coupler is decided by the phase difference (PD) between the even and odd mode while the input impedances of the two modes are matched perfectly [2]. Therefore the main difficulties in realizing a broadband FWDC are: (i) achieving broadband input impedance matching of the even and odd mode and (ii) keeping the PDs between the even and odd mode at a constant value during a broad frequency range. Several couplers have been proposed, such as the periodic shunt stubs along the coupled-line [3], [4], the microstrip coupled-line with pattern ground structure [2], [5]. They all contribute to the enhancement of PDs, but they are only used in narrow bandwidth applications because of their monotonously increased PDs. Asymmetrical coupler is another method to enhance the operational bandwidth, but the even- and odd-mode decomposition can not be used to analyze it [6], [7]. Therefore the analysis of asymmetrical coupler becomes more complicated.

In this paper, a broadband and symmetrical forward coupler is proposed. The even- and odd-mode Bloch impedances of the proposed FWDC can be designed to the values which are very close to 50 Ω. Therefore, the broadband impedance matching of the two modes can be achieved. The PDs between two modes also keeps approximately at a constant level within a broad frequency range. Due to these two characteristics, a FWDC can be designed with a broad bandwidth.

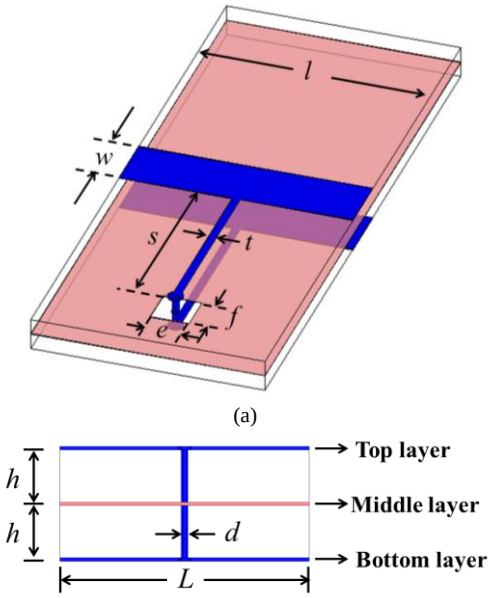


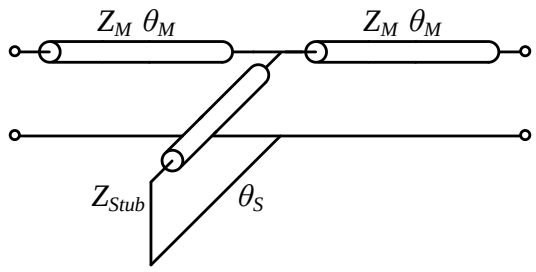
Fig. 1. (a) Unit cell of the proposed forward-wave directional coupler. (b) The front view.

II. Design Concept and Theoretical Modeling

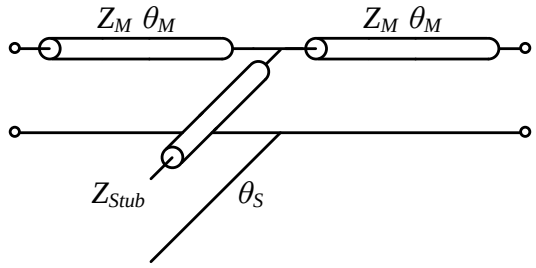
The proposed FWDC is designed based on the concept of periodic structures, and the configuration of the proposed unit cell is shown in Fig. 1. The middle layer in Fig. 1(a) is transparent to some degree so that the bottom layer with lighter color can be seen. As shown in Fig. 1, it is a three-layer structure and the middle layer serves as the reference plane. There are a transmission line and a stub at the center of the transmission line on the top layer. Besides, the pattern on the bottom layer is the same as the top layer, and they are connected with each other by a via at the end of the stubs. The width and length of the transmission line can be represented as w and l, respectively. The width of the shunt stub is t and the length is s. The thickness between each layer is represented as h and the diameter of the connecting via is d.

TABLE I
GEOMETRICAL DIMENSIONS AND THE CORRESPONDING PARAMETERS

Geometrical dimensions (mm)		Parameters of the equivalent models (at 2.5 GHz)
l = 18	e = 3.4	Z_M = 50 Ω
w = 1.8	f = 4.2	Z_{Stub} = 133 Ω
t = 0.16	h = 0.813	θ_M = 45°
s = 9.7	d = 0.28	θ_S = 45°



(a)



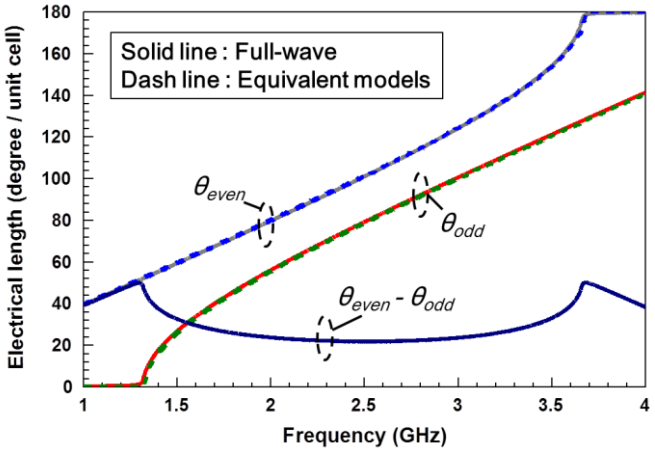
(b)

Fig. 2. Equivalent models of a unit cell (a) Odd mode. (b) Even mode.

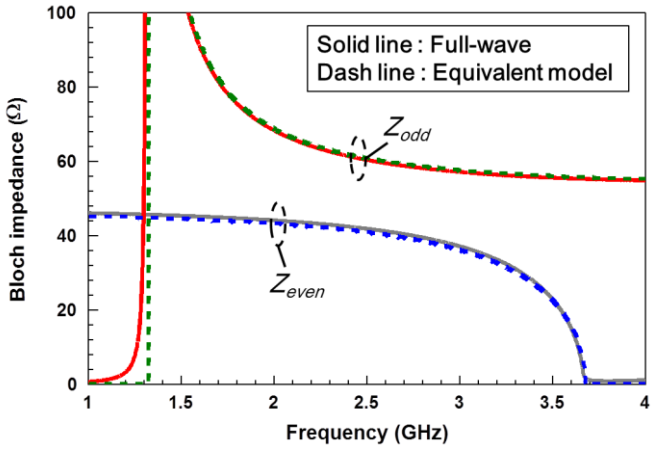
The rectangular hole which etches on the middle layer to ensure that the connecting via did not short to the middle layer is e in width and f in length. The geometrical dimensions of a unit cell are summarized in Table I.

Since the proposed structure is a symmetric structure, the even- and odd- mode decomposition can be used to synthesize it. The perfect electric conductor (PEC) plane and the perfect magnetic conductor (PMC) plane are placed on the plane of symmetry, the middle layer, for cases of the odd mode and the even mode, respectively. The equivalent models of both modes are shown in Fig. 2. As shown in Fig. 2(a), the odd-mode structure can be modeled as two sections of microstrip lines with characteristic impedances Z_M and electrical lengths θ_M and a short stub at the center. The stub is shorted to the reference plane because a PEC plane is placed on the middle layer. The corresponding characteristic impedance and electrical length of the short stub are Z_{Stub} and θ_S, respectively. The even-mode equivalent model is shown in Fig. 2(b). It is similar to the equivalent model of the odd mode except for the stub at the center. The stub is now an open stub because a PMC plane is placed on the middle layer. As shown in Fig. 2(b), the parameters using to represent the characteristic impedances and electrical lengths are the same as the odd mode. The extracted parameters are also summarized in Table I.

The even- and odd- mode electrical lengths and Bloch impedances of a unit cell are important for designing a periodic structure and they can be derived from the equivalent models by the Bloch-Floquet theorem [1]. The results are given as



(a)



(b)

Fig. 3. Simulation results for the (a) even- and odd-mode electrical lengths and (b) even- and odd-mode Bloch impedances.

$$\theta_{odd} = \cos^{-1}\left[\cos(2\theta_M) + \frac{r_z}{2}\sin(2\theta_M)\cot\theta_S\right] \quad (4a)$$

$$\theta_{even} = \cos^{-1}\left[\cos(2\theta_M) - \frac{r_z}{2}\sin(2\theta_M)\tan\theta_S\right] \quad (4b)$$

$$Z_{odd} = \frac{jZ_M\sin\theta_M\left[2\cos\theta_M + r_z\sin\theta_M\cot\theta_S\right]}{\sqrt{A+B}} \quad (4c)$$

$$Z_{even} = \frac{jZ_M\sin\theta_M\left[2\cos\theta_M - r_z\sin\theta_M\tan\theta_S\right]}{\sqrt{C-D}} \quad (4d)$$

$$A = \left[\left((r_z/2)\cot\theta_S\right)^2 - 1\right]\sin^2(2\theta_M) \quad (4e)$$

$$B = r_z\sin(2\theta_M)\cos(2\theta_M)\cot\theta_S \quad (4f)$$

$$C = \left[\left((r_z/2)\tan\theta_S\right)^2 - 1\right]\sin^2(2\theta_M) \quad (4g)$$

$$D = r_z\sin(2\theta_M)\cos(2\theta_M)\tan\theta_S \quad (4h)$$

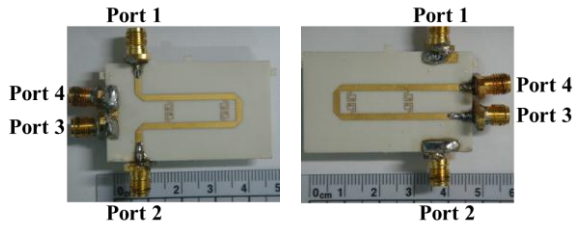
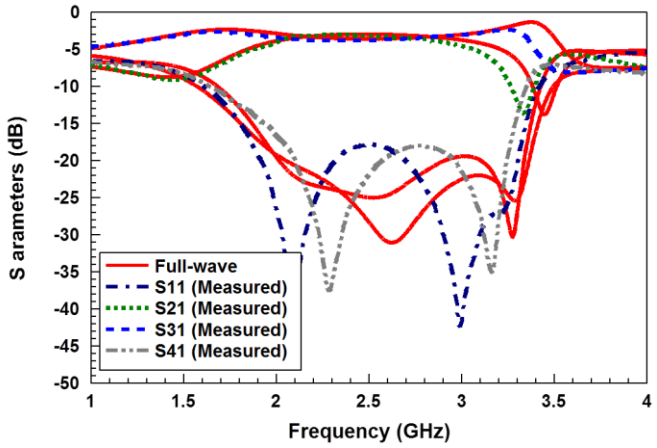
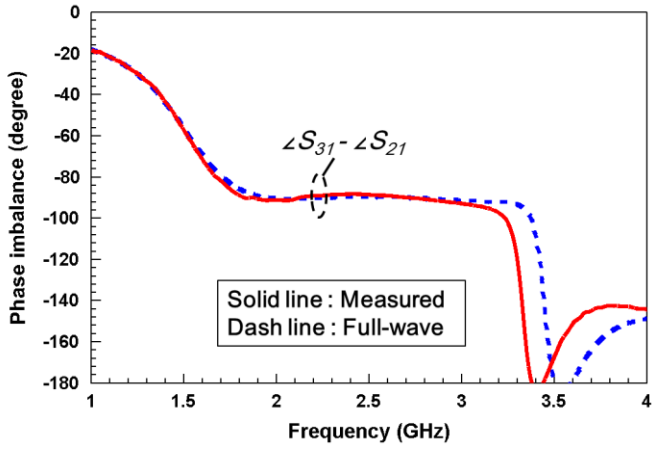


Fig. 4. Photographs of the fabricated 3-dB FWDC. (ε_r = 3.55)



(a)



(b)

Fig. 5. Measurement and full-wave simulation of the proposed 3-dB FWDC (a) S parameters and (b) phase imbalance.

where r_z is the impedance ratio and equals to Z_M/Z_{Stub}. The frequency dependence of θ_{odd} , θ_{even} , Z_{odd} , Z_{even} according to (4a)-(4d) are shown in Fig. 3. The full-wave simulation is also included for validation and they show good agreement. The values of the parameters of the equivalent models and the geometric dimensions used in the full-wave simulation can be found in Table I. As shown in Fig. 3(a), the phase of the even mode increases linearly with the frequency from 1 GHz to 3.3GHz and then increases faster near the cut-off frequency 3.7 GHz. The phase of the even mode keeps at 180 degree from 3.7 GHz to 4 GHz because the even-mode Bloch impedance becomes pure imaginary and corresponds to evanescent rather than propagating within this frequency range. The phase of the odd mode keeps at 0 degree from 1 GHz to 1.3 GHz for the same reason and starts to increase from the cut-off frequency 1.3 GHz. It also increases faster near the cut-off frequency and then turn to increases linearly from 1.7 GHz to 4 GHz. The coupling level of a FWDC is based on the PD of the two modes, so the PD is also plotted in Fig. 3(a). As shown in Fig. 3(a), the even- and odd- mode phases are parallel to each other from 1.7 GHz to 3.3 GHz. Therefore, the PD between the even and odd modes keeps at 22.5° within this frequency range. As demonstrated in Fig. 3(b), the even-mode Bloch impedance decreases gradually from 45 Ω to 0 Ω and there is a flat region from 1 GHz to 3.1 GHz where the impedance keeps approximately at 45 Ω. The odd-mode impedance also decreases gradually from 100 Ω to 55 Ω and keeps approximately at 57 Ω within a flat region from 1.9 GHz to 4 GHz. Because of these flat regions, the proposed structure can achieve good broadband matching. Recalling that two conditions to achieve a broadband FWDC are broadband constant PDs between the even and odd modes and broadband impedance matching. As demonstrated in Fig. 3, both conditions are achieved. As a result, a broadband FWDC can be expected.

III. Measured Results

A test sample of the proposed broadband 3-dB FWDC with the dimension shown in Table I is fabricated using Ro4003. The relative permittivity and loss tangent are 3.55 and 0.0027, respectively. The photographs and the port names are shown in Fig. 4. As shown in Fig. 4, the test sample is miniaturized by meandering the stubs and the total length is 28.51 mm (0.4 λg) excluding the additional structure for measurement. The measured and full-wave simulated scattering parameters are shown in Fig. 5(a), and they show good agreement. As shown in Fig. 5(a), the return loss and isolation are below -15 dB from 1.94 GHz to 3.28 GHz. Therefore, broadband matching is achieved. Moreover, the measured S_{21} and S_{31} are -3.8 ± 0.5 dB from 1.97 GHz to 2.85 GHz. The measured and simulated phase imbalance between port2 and port 3 are demonstrated in Fig. 5(b). They show good agreement except for the higher frequencies. This is because the glue used to connect between layers is FR4, the effect of loss become significant at higher frequencies. As shown in Fig. 5(b), the measured phase imbalance stays within -90° ± 2° from 1.78 GHz to 2.92 GHz.

IV. Conclusion

A novel broadband and compact FWDC is proposed. The broadband impedance matching of both the even- and odd-mode can be achieved. Besides, the phase difference between the even and odd modes can keep at a constant level within a broad frequency range. Therefore, a broadband FWDC can be designed. The measured S_{21} and S_{31} are -3.8 ± 0.5 dB from 1.97 GHz to 2.85 GHz and the corresponding fractional bandwidth is 37%.

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