Modeling of EBG Power Bus using Segmentation Method for GHz Noise Isolation

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Abstract

In this paper, we present a new modeling approach based on a segmentation method for noise isolations of a power bus in which partial electromagnetic bandgap (EBG) structures are embedded. When the EBG structure is inserted partially in the power bus, the stopband characteristics such as the cut-off frequencies and the noise isolation level are different from those predicted by the models assuming infinite EBG cells. The proposed modeling approach enables to predict the noise coupling coefficient of the partial EBG power bus accurately in the stopband as well as the passband. In the proposed modeling, the partial EBG power bus is divided into three segments of the partial EBG structures and the different size rectangular power/ground planes. The partial EBG structure is further divided vertically and modeled as the transmission line networks with via structure and a rectangular plane cavity model. The proposed modeling approach based on the segmentation method has been validated by good agreement between the modeling result and the electromagnetic simulation result.

1. INTRODUCTION

In the design of the highly integrated mixed-signal systems with fast edge rates and high switching frequencies, electromagnetic bandgap (EBG) structures have been studied as an efficient way to suppress the power/ground noise coupling and achieve the high noise isolation level in multi-layer printed circuit boards (PCBs). The partial EBG structures, especially, have recently been attracting attentions due to the small area, maintaining the power integrity characteristics and minimizing the effect of the reference plane on the signal lines [1]-[4].

In the partial EBG power bus, an EBG cell or a few EBG cells are placed locally on the port locations or the array of the EBG cells is inserted between the noise source and the victim. The small and finite numbers of the EBG cells in the partial EBG power bus guarantee the power integrity and the solid reference plane. However, due to the insufficient number of EBG cells there is no clear stopband in the partial EBG power bus. Therefore, the noise isolation level needs to be predicted cautiously for the partial EBG power bus. Most previous studies on the modeling of the EBG structure are focused on predicting the cut-off frequencies of the stopband [5]. It is difficult to apply the previous modeling approach to the partial EBG power bus to predict the noise isolation.

In this paper, we present a new modeling approach using segmentation method and a cavity model for the prediction of the noise isolation of the partial EBG power bus in multi-layer PCBs. The modeling approach provides a simple modeling and an accurate result. In the proposed modeling, the partial EBG power bus is divided into partial EBG structures and rectangular power/ground planes. The partial EBG structure is modeled as transmission line networks combined with a cavity model. The rectangular power/ground planes are modeled using cavity models. Finally, the noise coupling coefficient for the noise isolation prediction is obtained using the segmentation method with impedance matrices of each model.

2. SEGMENTATION METHOD FOR PARTIAL EBG POWER BUS

A partial EBG power bus with Z-shape EBG structures in multi-layer PCBs is introduced in [4]. It shows the wideband suppressions of noise coupling and high noise isolation level. We adopted the partial EBG power bus introduced in [4] for noise isolation modeling. The partial EBG

power bus consists of the irregular shaped power/ground planes and the four rectangular EBG patches as shown in Fig. 1. The Z-shape branches are formed in the center of the power plane. The EBG patches are embedded between the power plane and the ground plane. The EBG patches are connected with Z-shape branch through vias.

A. Segmentations of Partial EBG Power Bus

In the segmentation method an irregular structure can be considered as a combination of several simple parts based on the theory of Shelkunoff's equivalence principles [6]. We assume that the electric current sources are placed on both sides on the boundary of the segments and the tangential fields remain the same as the original partial EBG power bus. The couplings between the segments are ignored in the proposed modeling. Then, the partial EBG power bus can be divided into three parts which are rectangular power/ground planes and the partial EBG structure as shown in Fig. 1. The rectangular power /ground planes are the segment 1 and segment 3 which can be modeled as the rectangular cavities. Two partial EBG structures are in the segment 2. A partial EBG structure consists of a Z-shape branch, two EBG patches, and the corresponding ground plane. The Z-shape branch connects the power plane of segment 1 with the power plane of segment 3.
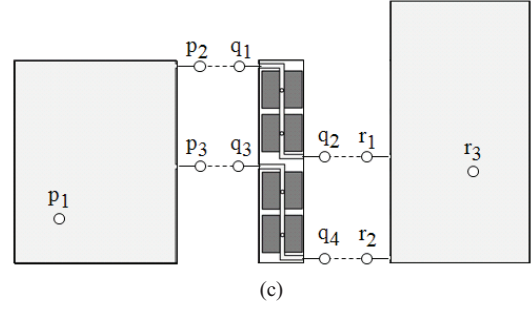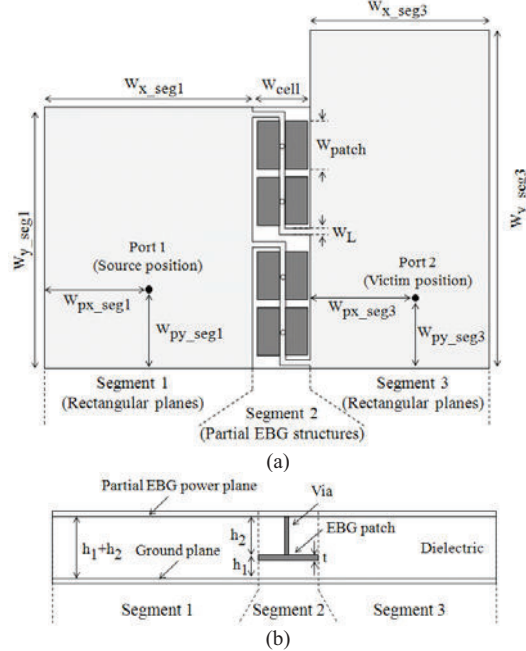

(a)

(b)

(c)

Fig 1. (a) Top view, (b) cross-sectional view of the partial EBG power bus and (c) the segmented partial EBG power bus for prediction of the noise isolation using segmentation method.

For the segments, we define the group of ports denoted as p, q, and r. The ports are defined vertically between the power plane and the ground plane. The segments are connected with the internal ports p_2, p_3, q_1, q_2, q_3, q_4, r_1, and r_2. The port pairs of (p_2, q_1) and (p_3, q_3) connect the rectangular cavity of the segment 1 with the partial EBG structure of the segment 2. The port pairs of (q_2, r_1) and (q_4, r_2) connect the partial EBG structure of the segment 2 with the rectangular cavity of the segment 3. The corresponding internal ports are connected to each other with holding the continuity of the current. The port p_1 and r_3 are the external ports. The corresponding ports of p_1 and r_3 are the port 1 and port 2, respectively in the original partial EBG power bus.

B. Impedance Matrices of Segmented Partial EBG Power Bus

All port voltages and currents of the segment 1 and the segment 3 are related by the impedance matrix, which can be obtained from the analytical impedance expressions using the cavity model [7]. The Z_p and Z_r which is the impedance matrix of the segment 1 and the segment 2 are given by,

$$Z_{p,ij} = j\omega\mu(h_1 + h_2)\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{C_m^2 C_n^2}{W_{x\_seg1}W_{y\_seg1}(k_{p,xm}^2 + k_{p,yn}^2 - k^2)}$$

$$\times \cos(k_{p,xm}x_{p,i})\cos(k_{p,yn}y_{p,i})\cos(k_{p,xm}x_{p,j})\cos(k_{p,yn}y_{p,j})$$

(1)

and

$$Z_{r,ij} = j\omega\mu(h_1 + h_2)\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{C_m^2 C_n^2}{W_{x\_seg3}W_{y\_seg3}(k_{r,xm}^2 + k_{r,yn}^2 - k^2)}$$

$$\times \cos(k_{r,xm}x_{r,i})\cos(k_{r,yn}y_{r,i})\cos(k_{r,xm}x_{r,j})\cos(k_{r,yn}y_{r,j})$$

(2)

where the index i and j represents the port number 1,2, and 3. The m and n represents the mode number associated with the cavity size. The x_p, y_p, x_r, and y_r are the locations of the ports. The other terms such as the constant C_m, C_n, and the wave number k are explained in [7].

The segment 2 consists of two identical partial EBG structures. The impedance matrix Z_q of the segment 2 is partitioned into submatrices. Then,

$$Z_q = \begin{bmatrix} Z_{e,11} & Z_{e,12} & 0 & 0 \\ Z_{e,21} & Z_{e,22} & 0 & 0 \\ 0 & 0 & Z_{e,11} & Z_{e,12} \\ 0 & 0 & Z_{e,21} & Z_{e,22} \end{bmatrix}$$

(3)

where $Z_{e,ij}$ (i,j=1,2) is the matrix entry of the impedance matrix Z_e for a partial EBG structure which will be derived in the next section. The total impedance matrix Z_t of the segmented partial EBG power bus is expressed in terms of each matrix of the segments as shown in Fig. 2.
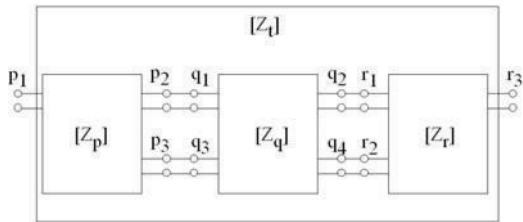

Fig. 2. Impedance matrices of the segmented partial EBG power bus.

The impedance matrix Z_t can be found using the impedance matrix equations in [8]. The impedance matrix equation introduced in [8] enables to eliminate the internal ports and find the impedance matrix with only external ports. When we obtain the impedance matrix Z_t, then the noise coupling coefficient S_{21} can be calculated from Z_t using the simple equation in [9].

3. MODELING OF PARTIAL EBG STRUCTURE

As mentioned in the introduction, it is important to predict the noise isolation level in the partial EBG power bus. The modeling of the partial EBG structure is crucial to the noise isolation level. The partial EBG structure consists of the bended transmission lines and the EBG cells as shown in Fig. 3 (a). The EBG cell consist of the narrow branch on the power plane, the EBG patch, and the corresponding ground plane as shown in Fig. 3 (b).
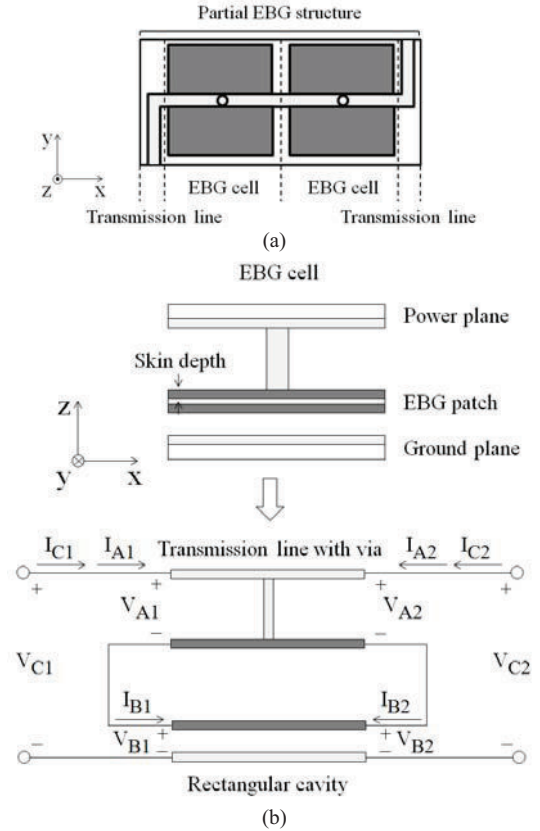

Fig. 3. (a) Top view of the partial EBG structure and (b) cross-sectional view and vertical segmentation of the EBG cell

In multi-layer PCBs, the skin depth is usually smaller than the metal thickness of the EBG patch over MHz frequencies and the noise cannot propagate inside the EBG patch vertically. So, we can ignore the vertical coupling through the EBG patch. Then, the EBG patch can be divided into two patches which connect at edge. Due to the separated EBG patches, the EBG cell can be divided vertically into the transmission line networks with a via and the rectangular cavity. The narrow branch connecting the upper plane of the segmented EBG patch through a via forms the transmission line networks with a via. The lower plane of the segmented EBG patch and the corresponding ground plane form the rectangular cavity. A noise current should detour the surface of the EBG patch at edges because it can only flow on the surface of the EBG patch. The upper EBG patch and the lower EBG patch are connected at the edge. We define the port A_1, A_2, B_1, B_2, C_1, and C_2 as shown in Fig. 3 (b). The impedance matrix Z_c can be obtained in terms of Z_a and Z_b, then

$$Z_c = \begin{bmatrix} Z_{a,11} + Z_{b,11} & Z_{a,12} + Z_{b,12} \\ Z_{a,21} + Z_{b,21} & Z_{a,22} + Z_{b,22} \end{bmatrix}$$

(4)

To find the impedance matrix Z_a of the transmission line networks with a via, the ABCD matrix is used. The transmission line networks with a via can be modeled into a combination of transmission lines and inductance as shown in Fig. 4.
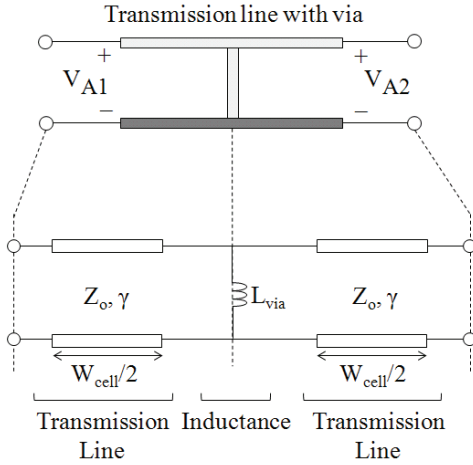

Fig. 4. The ABCD matrix model of the transmission line networks with a via.

The total ABCD matrix can be calculated from the result of the equations below.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma \cdot \dfrac{W_{cell}}{2}) & Z_o \sinh(\gamma \cdot \dfrac{W_{cell}}{2}) \\ \dfrac{1}{Z_0}\sinh(\gamma \cdot \dfrac{W_{cell}}{2}) & \cosh(\gamma \cdot \dfrac{W_{cell}}{2}) \end{bmatrix}$$

$$\times \begin{bmatrix} 1 & 0 \\ \dfrac{1}{j\omega L_{via}} & 1 \end{bmatrix} \begin{bmatrix} \cosh(\gamma \cdot \dfrac{W_{cell}}{2}) & Z_o \sinh(\gamma \cdot \dfrac{W_{cell}}{2}) \\ \dfrac{1}{Z_0}\sinh(\gamma \cdot \dfrac{W_{cell}}{2}) & \cosh(\gamma \cdot \dfrac{W_{cell}}{2}) \end{bmatrix}$$

(5)

where Z_O is the characteristic impedance. The γ represents the propagation constant. The ABCD matrix can be converted into the impedance matrix Z_a using the equations in [9]

The impedance matrix Z_b is obtained using the resonant cavity model. The rectangular cavity is formed by the EBG metal patch and the corresponding ground plane. The width of the rectangular cavity is W_{patch} and the height is h_1.

The ports are located at the center of the edges. Then, the impedance matrix Z_b is given by,

$$Z_{b,ij} = j\omega\mu h_1 \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{C_m^2 C_n^2}{(W_{patch})^2(k_{b,xm}^2 + k_{b,yn}^2 - k^2)}$$

$$\times \cos(k_{b,yn}\frac{W_{patch}}{2})\cos(k_{b,xm}W_{patch})\cos(k_{p,yn}\frac{W_{patch}}{2})$$

(6)

The total impedance matrix of the partial EBG structure is obtained and this impedance matrix is equal to the impedance matrix Z_e. Finally, we can find the impedance matrix Z_t for the noise isolation of the partial EBG power bus.

4. MODEL VALIDATION

To validate the proposed modeling, the noise coupling coefficient calculated from the proposed model is compared with the electromagnetic (EM) simulation result using Ansoft SIWAVE. The noise coupling coefficient S_{21} is compared in the frequency range from 0.1GHz to 10GHz. The simulation structure consists of three layers which are the power plane layer, the EBG patch layer, and the ground plane layer. The lossy FR-4 (loss tangent: 0.02) is used as a dielectric material. The copper is used as the metal, the conductivity of which is 5.8×10^7S/m. The simulation structure and dimensions for the validation of the model are shown in Fig. 5 and Table 1, respectively.
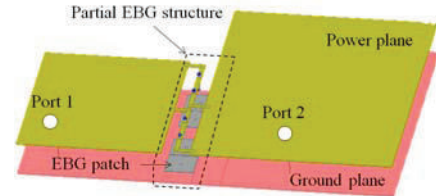

Fig. 5. The simulation structure for the model validation

TABLE 1

DIMENSIONS AND DESIGN PARAMETERS FOR THE VALIDATION

OF THE MODEL

Design parameters and Dimensions			(Unit: mm)
W_{x_seg1}	20	W_{y_seg1}	22
W_{x_seg3}	28	W_{y_seg3}	36
W_{px_seg1}	5	W_{py_seg1}	4
W_{px_seg3}	9	W_{py_seg3}	12
W_{cell}	4.2	W_{patch}	4
W_L	0.6	t	0.018
h_1	0.1	h_2	0.8

Fig. 6 depicts the calculated result using the proposed modeling approach and the EM simulation result. As shown in Fig. 6, the proposed modeling approach successfully predicts the resonance peaks and the noise isolation level, compared to the EM simulation result.
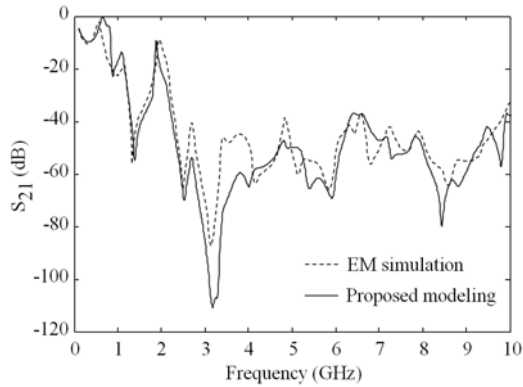

Fig. 6. The noise coupling coefficients which illustrate that good agreement validates the proposed modeling approach.

The proposed modeling approach for predicting the noise isolation level of the partial EBG power bus in multi-layer PCBs is validated by good agreements between the calculated result from the proposed model and the EM simulation result.

5. CONCLUSION

We have presented a new modeling approach based on a segmentation method using impedance matrices to predict the noise isolation of the partial EBG power bus. The proposed modeling approach provides the analytical model, the accurate result, and a simple modeling without the efforts to extract the equivalent circuit parameters of the partial EBG structure. The analytical model from the proposed modeling approach provides the accurate result and reduced the computational time, compared to the EM simulation result. Further to enhance the modeling, the coupling between the EBG patch and the segment 1, 3 can be included in the modeling, which causes the discrepancy of high-frequency peaks in the S_{21} result.

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Efficient Electromagnetic Simulation of Angled and Thin Structures by Using CFDTD and HIE-FDTD Methods

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Abstract

In this paper, we propose an effective electromagnetic simulation technique which is constructed by combining the conformal FDTD (CFDTD) method and the hybrid implicit-explicit (HIE)- FDTD method. The proposed technique can circumvent the above problems by exploiting advantages of the HIE-FDTD method and the CFDTD method.

1. Introduction

The finite-difference time-domain (FDTD) method is one of the powerful electromagnetic simulation techniques for solving Maxwell's equations. Since the FDTD method is based on the explicit time marching method, it has a limitation on the time step size related to the numerical stability condition. Concretely, the maximum time step size used in the simulation, Δt is selected so that the following Courant-Friedrichs-Lewy(CFL) condition is satisfied:

$$\Delta t \leq \frac{1}{v\sqrt{(\Delta x_{\min})^{-2} + (\Delta y_{\min})^{-2} + (\Delta z_{\min})^{-2}}} \quad (1)$$

where Δx_{min}, Δy_{min}, and Δz_{min} are minimum lengths of the Yee's cell in x, y, and z directions, respectively, and v is a maximum wave velocity in medium.

Fig. 1 shows the computer-aided design (CAD) model of an angled interconnection pattern on a printed circuit board (PCB). The object to be analyzed is discretized finely in x and y directions to approximate the angled interconnection pattern accurately. Hence, Δz becomes extremely small compared with those of other directions. As a result, these facts increase the total number of the cells, and require an extremely small time step size to satisfy (1).

In this paper, we propose an efficient electromagnetic simulation technique for the angled interconnection pattern on the PCB by exploiting the advantages of the CFDTD and HIE-FDTD methods. The advantages provide smaller number of cells and larger time step sizes.
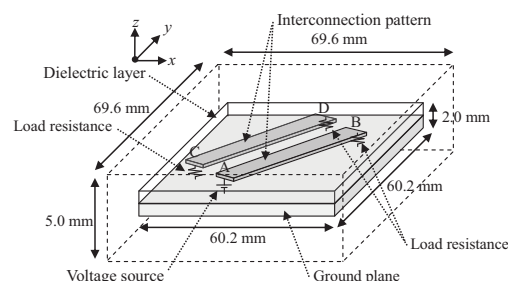

Fig. 1. CAD model of PCB, where two interconnection patterns are angled 30 degrees toward x axis.
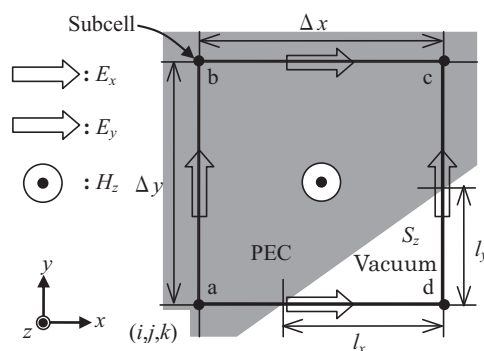

Fig. 2. Electromagnetic fields arrangement in the vicinity of PEC.

2. Conventional methods

The CFDTD method employs a subcell scheme instead of the standard Yee's cell method for the discretization of the angled pattern which are shown in Fig. 2. [1] shows that the subcell is easily exploited by including parameters of the subcell into the coefficients of updating formulas in the conventional FDTD method. Because of these characteristics, the CFDTD method is effective for the simulation of the

complicated structure compared with the conventional FDTD method.

The HIE-FDTD method employs the hybrid implicit-explicit finite difference scheme[2], which is different from the one used in the conventional FDTD method, to approximate a differential operator with respect to time. Concretely, if the object to be analyzed is discretized finely in z direction, the differential operator with respect to time in z direction is discretized implicitly. As a result, in the HIE finite difference scheme, the minimum cell size is free from (1) as shown below:

$$\Delta t_{HIE} \le \frac{1}{v\sqrt{(\Delta x_{\min})^{-2} + (\Delta y_{\min})^{-2}}} \qquad (2)$$

3. Proposed method

In this section, we formulate the efficient electromagnetic simulation technique by exploiting the advantages of the CFDTD and HIE-FDTD methods. In the proposed method, not only the subcell is used for x and y directions but also the hybrid implicit-explicit finite difference scheme is applied to the differential operator with respect to time in z direction. Therefore, Δx_{min} and Δy_{min} can be enlarged, and the time step size is determined by (2) similarly to the HIE-FDTD method.

In order to generate updating formulas, we focus on the feature of the CFDTD method as mentioned in [1]. The updating formula is led in a vector-matrix form:

$$K_1 \cdot u^{n+1} = K_2 \cdot u^n \qquad (3)$$

where n denotes a time index, and u is the unknown vector composed of electric and magnetic field vectors as shown in [3]. K_1 includes the parameters of the subcell defined in the CFDTD method. Additionally, these values are stamped to the same positions in a coefficient matrix of the HIE-FDTD method. As a result, the computational complexity of the proposed method is the same as that of the HIE-FDTD method.

4. Numerical result

we applied the proposed method to the angled interconnection pattern illustrated in Fig. 1 to estimate the accuracy and the efficiency of our approach. The details of
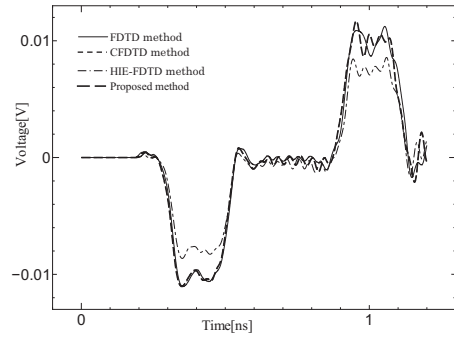

Fig. 3.   Waveform results at D in Fig. 1.

example circuit are shown in [3].

The waveform results at the observation point D is illustrated in Fig. 3. Because of using the subcell scheme, the results of the CFDTD method and the proposed method agree with those of the FDTD method. This means that the proposed method can obtain the accurate result even if the coarse grid is employed. Additionally the proposed method is about 42.8 times faster than the FDTD method. As a result, the proposed method is more effective than the conventional methods for the simulation of the angled interconnection pattern on the PCB.

5. Conclusion

In this paper, the efficient electromagnetic simulation technique has been developed for the analysis of the angled interconnection pattern on the PCB based on the CFDTD method and the HIE-FDTD method.

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Three Types of Interconnect Analysis Schemes Based on Latency Insertion Method

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Abstract

This paper describes three types of interconnect analysis schemes based on the latency insertion method (LIM). First, some features and the limitation of the time step size for the LIM are described. Next, to overcome the inherent problems and expand the applicable scope of the LIM, three types of improved schemes are developed. Finally, numerical results show that our methods are useful and efficient for the simulations of large interconnect networks.

1. Introduction

Significant advances of the semiconductor packaging technology have provided complicated designs of high-speed and high-density electronic circuits. Various effects related to the high-frequency characteristics of signals induce unexpected behaviors, such as signal delay, reflection, and crosstalk, which directly degrade the signal integrity of interconnect networks on a printed circuit board (PCB). In order to deal with detailed behaviors of those effects, equivalent circuits of the interconnects tend to be composed of a large number of linear elements. These facts force a large amount of simulation cost for a conventional SPICE-like simulator, and therefore, some kind of fast and accurate simulation method is strongly needed.

The latency insertion method (LIM) is one of the finite difference time domain (FDTD)-based transient analysis methods for the fast simulation of the large interconnects [1]. However, since the LIM is based on the explicit method, it has a limitation on the time step size to satisfy the numerical stability condition shown in [1].

In this paper, in order to overcome the limitation of the LIM, three types of improved LIM are described.
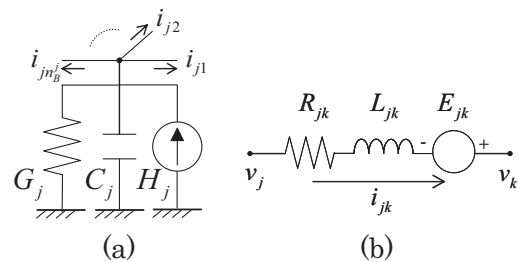

Fig. 1. Network topologies required for the LIM. The arrow corresponds to the direction of branch current. (a) Node topology; a parallel combination of the grounded capacitance C_j, the conductance G_j, and the independent current source H_j. (b) Branch topology; a serial combination of the inductance L_{jk}, the resistance R_{jk}, and the independent voltage source E_{jk}.

The remainder part of the paper is organized as follows. In Section II, the conventional LIM is reviewed. Section III, IV, and V describe the concepts and the features of the ADE-LIM, the PC-LIM, and the LILIM. Finally, conclusions are described in Section V.

2. Basic LIM

The LIM is one of the fast and powerful circuit simulation techniques based on the explicit leapfrog scheme [1]. The LIM assumes that a network to be analyzed is composed of the node and the branch topologies shown in Fig 1.

First, the Kirchhoff's current law (KCL) and the Kirchhoff's voltage law (KVL) are applied to the node topologies and the branch topologies in the network, and the following equation

$$C_j \frac{dv_j}{dt} + G_j v_j = -\sum_{k=1}^{n_B^j} i_{jk} + H_j \ , \qquad (1)$$

$$L_{jk} \frac{di_{jk}}{dt} + R_{jk} v_{jk} = v_j - v_k + E_{jk} \ , \qquad (2)$$

are derived. Then, by applying the finite difference method based on the leapfrog scheme to (1) and (2), the updating formulas of the node voltage and the branch current are lead as

$$v_j^{n+\frac{1}{2}} = \frac{C_j}{C_j + \Delta t G_j} v_j^{n-\frac{1}{2}}$$
$$+ \frac{\Delta t}{C_j + \Delta t G_j} \left(-\sum_{k=1}^{n_B^j} i_{jk}^n + H_j^n \right), \qquad (3)$$

$$i_{jk}^{n+1} = \frac{L_{jk} - \Delta t R_{jk}}{L_{jk}} i_{jk}^n$$
$$+ \frac{\Delta t}{L_{jk}} \left(v_j^{n+\frac{1}{2}} - v_k^{n+\frac{1}{2}} + E_{jk}^{n+\frac{1}{2}} \right), \qquad (4)$$

where n and Δt indicate the time index and the time step size. Note that each of the voltage and current variables is arranged alternately in every half time step due to the leapfrog scheme. Thus, the LIM can perform the fast and accurate analysis compared with the matrix-based SPICE-like simulators.

Since the LIM is based on the explicit method, it has the limitation on the time step size to satisfy the numerical stability condition similar to the CFL one. Concretely, the maximum time step size of the LIM, Δt_{max}, has the following upper bound [1,2]:

$$\Delta t_{\max} < \sqrt{2} \min_{j=1}^{n_N} \left(\sqrt{\frac{C_j}{n_B^j} \min_{m=1}^{n_B^j} (L_{jm})} \right), \qquad (5)$$

where n_B^j is the number of the branches connected to the node j, L_{jm} is the value of the inductor in the m-th branch connected to the node j, and C_j is the value of the grounded capacitor connected to the node j. Clearly, Δt_{max} is limited by the minimum value of the reactive elements in the circuit. Therefore, if the small and fictitious elements are inserted into the circuit, Δt_{max} becomes extremely small, and the simulation cost increases significantly.
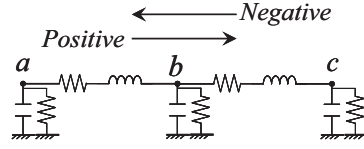

Fig. 2. Example circuit.

3. ADE-LIM

In order to overcome the limitation of the time step size, we consider to introduce the ADE scheme [3] and propose the ADE-LIM [4, 5], which contains two updating steps, namely, *Positive* and *Negative*. Fig. 2 shows the example circuit to explain the updating steps. In Fig. 2, the ADE method is applied to the KCL equation obtained from the node b, then, the following differential equation is led as

$$v_{P,b}^{n+1} = \frac{C_b}{C_b + \Delta t G_b} v_b^n + \frac{\Delta t}{C_b + \Delta t G_b} \left(i_{P,ab}^{n+1} + i_{bc}^n \right), \qquad (6)$$

where P denotes the Positive. Then, the implicit difference equation of (2) based on the backward Euler method is substituted into i^{n+1} in (6). This treatment leads the following updating formula,

$$\left(1 + \beta_b^- \alpha_{ab}^- \right) v_{P,b}^{n+1} - \beta_b^- \alpha_{ab}^- v_{P,a}^{n+1} =$$
$$\beta_b^+ v_b^n + \beta_b^- \alpha_{ab}^+ i_{ab}^n - \beta_b^- i_{bc}^n, \qquad (7)$$

where α and β are the coefficients. Equation (7) provides the explicit expression for the unknown voltage if updating is performed from left to right in Fig. 2. On the other hand, the updating formula in Negative is easily derived based on that of the Positive.

In the ADE-LIM, updating the voltages and the currents is performed twice in per time step. Thus, the computational complexity increases compared with that of the basic LIM. However, the ADE-LIM employs the larger time step size than the basic LIM. As a result, the ADE-LIM can perform the fast circuit simulation.

4. PC-LIM

The LIM requires the reactance elements to derive the updating formulas. Thus, if the network is composed of the node without capacitance or the branch without inductance, the small value of capacitance / inductance must be inserted into the ill-constructed topologies. However, this treatment leads the extremely small time step size because the

time step size is deeply dependent on the reactance elements shown in (5). To overcome this inherent problem, we proposed the predictor-corrector (PC)-LIM [6]. The PC-LIM employs a large value of the fictitious element instead to the small value. This treatment relaxes the limitation of (5).

In order to generate the updating formula for the ill-constructed branch, first, the large value of the fictitious inductance L_{ab}^f is inserted into the branch as shown in Fig. 3 (b). In Fig. 3 (b), the following predictor updating formula is derived,

$$\hat{i}_{sb}^{n+1} = \frac{L_{ab}^f - \Delta t R_{ab}}{L_{ab}^f} i_{ab}^n + \frac{\Delta t}{L_{ab}^f}\left(v_b^{n+\frac{1}{2}} - v_b^{n+\frac{1}{2}} \right). \quad (8)$$

The current i_{ab}^{n+1} updated by (8) is not the correct solution. In order to improve the accuracy of the inaccurate value, extra updating is performed by exploiting a compensation voltage source. Then, the following corrector updating formula is led as

$$i_{sb}^{n+1} = \frac{L_{ab}^f - \Delta t R_{ab}}{L_{ab}^f} i_{ab}^n$$

$$+ \frac{\Delta t}{L_{ab}^f}\left(v_b^{n+\frac{1}{2}} - v_b^{n+\frac{1}{2}} + \hat{E}_{ab}^{n+\frac{1}{2}} \right), \quad (9)$$

where

$$\hat{E}_{ab}^{n+\frac{1}{2}} = L_{ab}^f \frac{di}{dt} \approx L_{ab}^f \frac{\hat{i}_{ab}^{n+1} - i_{ab}^n}{\Delta t} \quad . \quad (10)$$

In the proposed PC-LIM, the unknown current in the ill-constructed branch is updated by (8). After that, the compensation voltage source is generated by (10). Finally, to improve the accuracy of the inaccurate value, (9) is calculated.

The most important property of the above predictor-corrector updating algorithm is that it retains the leapfrog time-marching scheme of the basic LIM. In addition, since the large fictitious latency is exploited in the predictor and the corrector, the maximum time step size is not strictly limited by (5) compared with the basic LIM. Moreover, because the predictor and the corrector are performed only for the ill-constructed topologies, difference of the computational complexity between the proposed method and the basic LIM is slight.
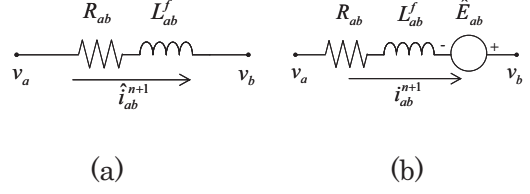

(a) (b)

Fig. 3. Circuit representation. (a) Predictor updating. (b) Corrector updating.
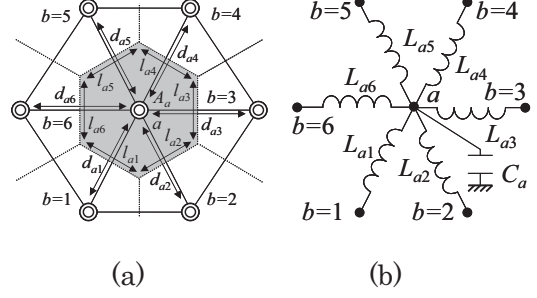

(a) (b)

Fig. 4. Voronoi diagram and triangular mesh for conductor media. (a) Double circle, dashed lines, and solid lines indicate the Voronoi point, the Voronoi region, and triangular meshes. (b) Equivalent circuit, where the grounded resistance G and the serial resistance R are not depicted.

5. LIM with Triangular Mesh

For modeling of the arbitrary shaped PDN, square meshes must be tiny because the PDN contains the fine structures. This fact leads that the number of unknown variables increases drastically. Additionally, the square mesh suffers from the staircase approximation on the edge of the geometric structure. To cope with the above inherent problems, the efficient modeling methods based on triangular mesh have been proposed [7]. These methods successfully reduce the total number of unknowns without degrading the accuracy because the triangular mesh scheme is flexible to capture the complex structures by resizing the mesh sizes locally. These triangular meshes are lead by Delaunay Triangularization and Voronoi Tessellation as shown in Fig. 4(a). In Fig. 4(a), the gray hexagonal part, d_{ab}, and l_{ab} indicate the area of Voronoi region A_a surrounding Voronoi point a, the length of the Voronoi edge, and the length of the edge in the triangular mesh, respectively. The equivalent circuit is extracted from the object meshed triangularly, as shown in Fig. 4(b), where the Voronoi point and the Voronoi edge correspond to the node and the branch topologies assumed by the LIM. The

equivalent circuit is composed of the grounded capacitances and the serial inductances, thus the LIM is directly applied to the equivalent circuit extracted from triangular meshes.

6. Numerical Results

In order to estimate the efficiency of the proposed methods, the example circuit has been simulated by the basic LIM and the ADE-LIM. The example circuit is illustrated in Fig. 5, which is composed of 128 transmission lines, and each transmission line consists of 10 unit segments. Each of the unit segments is the π model constructed by R (= 0.2 Ω), L (= 0.1 nH), C (= 0.1 pF), and G (= 0.001 S). Additionally, the values of the mutual inductances and the mutual capacitances are Lm = 1.0 pH, and Cm = 1.0 fF, respectively. In this case, the maximum time step size used in the LIM, Δt_{max}, is equal to 3.162 ps, which is less than the upper bound obtained by (5). The input current sources H_{in1} and H_{in2} are connected at the input points A and B in Fig 5, respectively. These are the same trapezoidal pulse, of which the pulse value is 0.033 A, rise and fall times are 0.1 ns, the pulse width is 5 ns, and the period is 10.2 ns, except for the delay times of 1.0 ns and 1.4 ns, respectively. The simulation interval is [0 ns, 30 ns].

The waveform results at the observation points C and D are illustrated in Fig. 6. The waveform from the ADE-LIM with Δt_{max} agrees well with the exact result by the LIM and HSPICE. Furthermore, it is confirmed that the numerical stability of the ADE-LIM is much superior to the LIM though the accuracy of the ADE-LIM with $7\Delta t_{max}$ is slightly degraded compared with the LIM.

Table I shows the CPU times and speed-up ratios, and indicates that the ADE-LIM with $7\Delta t_{max}$ is about 3.6 and 36 times faster than the LIM and the HSPICE, respectively. As a result, it is confirmed that the proposed method is more effective than the conventional methods for the tightly coupled transmission lines analysis.

7. Conclusions

In this paper, three types of interconnect analysis schemes have been described. The
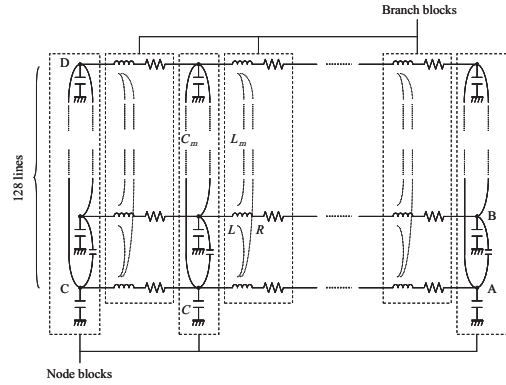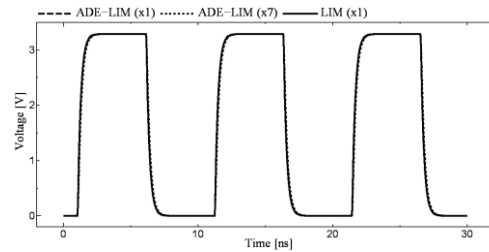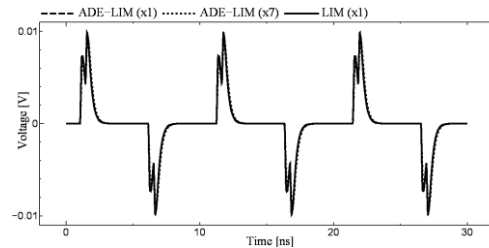

Fig. 5. Tightly coupled transmission lines, each of which is composed of 11 node blocks and 10 branch blocks. This network includes 174656 circuit elements.

(a)

(b)

Fig. 6. Waveform results at (a) C, and (b) D in Fig. 6.

TABLE I
COMPARISON OF CPU TIMES.

Method	CPU Time [s]	Speed-up LIM (x1)	HSPICE
HSPICE	8146	*	1.00
LIM (x1)	794.58	1.00	10.25
ADE-LIM (x1)	1549.58	0.51	5.25
ADE-LIM (x3)	516.03	1.53	15.78
ADE-LIM (x5)	313.16	2.53	26.02
ADE-LIM (x7)	221.11	3.59	36.84

first and the second approaches can do the fast transient simulations by overcoming the inherent problems of the basic LIM. the third one is the modeling method which enables to apply the LIM to general structures.

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Modeling and Circuit/Electromagnetic Simulations of EMC Problems Based on Leapfrog Scheme

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Abstract

This paper describes two different methods based on an explicit leapfrog scheme. The first one is a fast circuit simulation technique obtained by applying a model order reduction (MOR) technique to the block latency insertion method (block-LIM). The block-LIM is significantly-fast in the simulation of tightly coupled networks, and we further accelerate it by means of the MOR technique. The second one is a full-wave transient simulation technique based on the retarded partial element equivalent circuit (PEEC) method and the leapfrog scheme. The network realized by a nonretarded PEEC method is often solved by a modified nodal analysis in conjunction with a direct solver. In contrast, we apply the leapfrog scheme to the time domain formulation of a retarded PEEC network instead of the conventional solver. The simulation results of example problems show that the leapfrog-based techniques are suitable for the fast circuit/electromagnetic simulations in the time domain.

1. Introduction

Advances of a semiconductor packaging technology have induced high-density integrated circuits (ICs), where an extremely small area is filled up with billions of switching devices. Therefore, development of simulation techniques for the recent advanced packaging technology is becoming more and more challenging due to difficulties in modeling the complicated phenomena arising in interconnects. The difficulties are caused by geometrically-complicated structures, which obscure exact causality of electromagnetic behaviors of interest. Because any simulation technique simplifies and approximates those real phenomena in the modeling process, it is strongly required to understand their right meanings to deal with them properly.

In this paper, we propose two different simulation techniques based on an explicit leapfrog scheme. The leapfrog scheme is one of the explicit finite difference methods in the time domain and has an advantage over conventional matrix-based simulators in computational cost. First, we apply a model order reduction (MOR) technique to the block latency insertion method (block-LIM) [1] to achieve the fast circuit simulation of multiconductor transmission lines (MTLs) with nonlinear devices. On the other hand, we apply the leapfrog scheme to the retarded partial element equivalent circuit (PEEC) model [2] to perform the full-wave simulation in the time-domain. In contrast to conventional direct solvers, the time marching procedure of the leapfrog scheme is completely explicit: a matrix inversion or triangular factorization is not needed.

The remainder part of the paper is organized as follows. In Section 2, we propose the combined block-LIM and MOR technique and show the simulation results related to the MTLs with CMOS inverters. Then, the application technique of the leapfrog scheme to the retarded PEEC network is discussed in Section 3. We demonstrate availability and efficiency of the proposed leapfrog-based PEEC solver by performing an example simulation of interconnects. After that conclusions are given in Section 4.
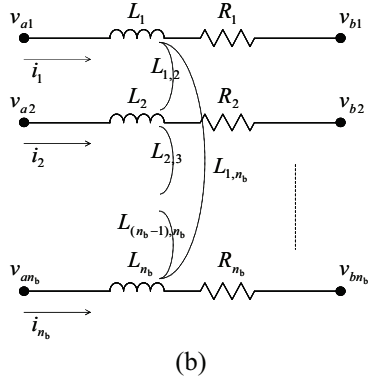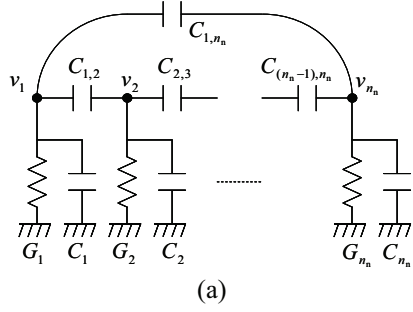
(a)

(b)

Fig. 1. Tightly coupled blocks defined in the block-LIM. (a) A node block, in which n_n nodes are connected through mutual capacitances. (b) Branch block topology, in which n_b branches are connected through mutual inductances.

2. Model Order Reduction Technique Applied to the Block-LIM

In the block-LIM, a part in which the nodes are connected with each other through mutual capacitances is defined as the node block shown in Fig. 1(a). In addition, another part that contains the branches connected with each other through mutual inductances is categorized as the branch block shown in Fig. 1(b). Formulation for the block-LIM begins with applying the Kirchhoff's current law (KCL) to the node block and the Kirchhoff's voltage law (KVL) to the branch block. Subsequently, the leapfrog scheme is applied to the KCL and KVL equations to derive the difference equations associated with them. Finally, transforming the difference equations leads to the following updating formulas of the node voltages and branch currents in the

blocks.

$$\left(\frac{1}{\Delta t}\mathbf{C}_a + \mathbf{G}_a\right)\mathbf{v}_a^{n+\frac{1}{2}} = \frac{1}{\Delta t}\mathbf{C}_a\,\mathbf{v}_a^{n-\frac{1}{2}} - \tilde{\mathbf{i}}_a^{\,n}, \quad (1)$$

$$\frac{1}{\Delta t}\mathbf{L}_{ab}\,\mathbf{i}_{ab}^{n+1} = \left(\frac{1}{\Delta t}\mathbf{L}_{ab} - \mathbf{R}_{ab}\right)\mathbf{i}_{ab}^{n} - \mathbf{v}_{ab}^{n+\frac{1}{2}}, \quad (2)$$

where n is the time index, Δt is the time step size, and the bold characters represent the matrices and vectors defined in [1].

The macromodels of the node and branch blocks are obtained by applying the passive reduced-order interconnect macromodeling algorithm (PRIMA) to each block. In the PRIMA, by using the block Arnoldi algorithm, we generate the projection matrix $\mathbf{V}_q$, where q is the order of the reduced model. Then, deriving the reduced linear system using $\mathbf{V}_q$ and applying the leapfrog scheme to the system of the node block, for instance, lead to

$$\left(\frac{1}{\Delta t}\tilde{\mathbf{C}} + \tilde{\mathbf{G}}\right)\mathbf{z}_a^{n+\frac{1}{2}} = \frac{1}{\Delta t}\tilde{\mathbf{C}}\,\mathbf{z}_a^{n-\frac{1}{2}} - \tilde{\mathbf{B}}\mathbf{u}^n, \quad (3)$$

where $\mathbf{z} = \mathbf{V}_q^{\mathrm{T}}\mathbf{v}_a$ is the reduced state vector of size q and

$$\tilde{\mathbf{G}} = \mathbf{V}_q^{\mathrm{T}}\mathbf{G}_a\mathbf{V}_q, \quad \tilde{\mathbf{C}} = \mathbf{V}_q^{\mathrm{T}}\mathbf{C}_a\mathbf{V}_q, \quad \tilde{\mathbf{B}} = \mathbf{V}_q^{\mathrm{T}}\mathbf{B}, \quad (4)$$

where $\mathbf{B}$ is the incident matrix representing contributions of the input and output values.

The example circuit is the MTLs with CMOS inverters illustrated in Fig. 2. The MTLs are composed of the branch and node blocks which are alternately connected in series. We consider that the MTLs consist of 128 transmission lines divided into 50 segments so that there exist the 50 linear branch blocks and 49 linear node blocks. Two pulse signal generators are appended to the leftmost nodes of the MTLs, respectively, and we observe the waveform results of the voltages at the far end of the top line.

In Fig. 3, it is confirmed that the waveforms obtained from the proposed method with the 40th order macromodel are almost completely agree with those from the original block-LIM. In the case of $q = 40$, the proposed method can simulate about 13.6 times faster than the original block-LIM.
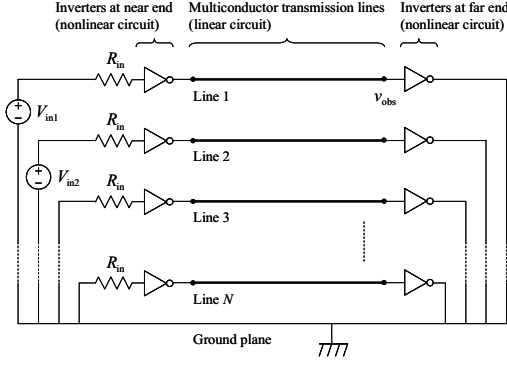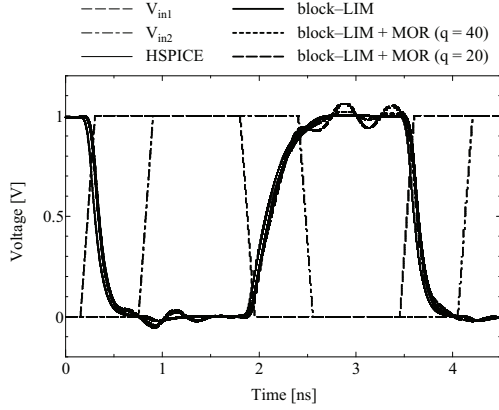
Fig. 2. MTLs with CMOS inverters.

Fig. 3. Waveform results for far end of the driving line in Fig. 2.

3. Full-Wave PEEC Time Domain Solver Based on Leapfrog Scheme

Derivation of the retarded PEEC model begins with the following time-dependent potential function inside a conductor

$$\mathbf{E}(\mathbf{r},t) = -\frac{\partial \mathbf{A}(\mathbf{r},t)}{\partial t} - \nabla \Phi(\mathbf{r},t) + \mathbf{E}_{\text{inc}}(\mathbf{r},t), \; (5)$$

where $\mathbf{E}$ is the electric field in the conductor, $\mathbf{A}$ and Φ are the vector and scalar potentials, $\mathbf{E}_{\text{inc}}$ is the incident electric field, and r is the position vector. Then, the structure to be analyzed is descretized into N_V volume cells and N_S surface cells. Next, to perform the Galerkin procedure, we approximate (5) with pulse basis functions, multiply the resultant equation by a weighting function, and integrate it over volume V_α. In this procedure, the weighting function is the same as the basis function. Finally, we get the equation related to the current I_α flowing through the
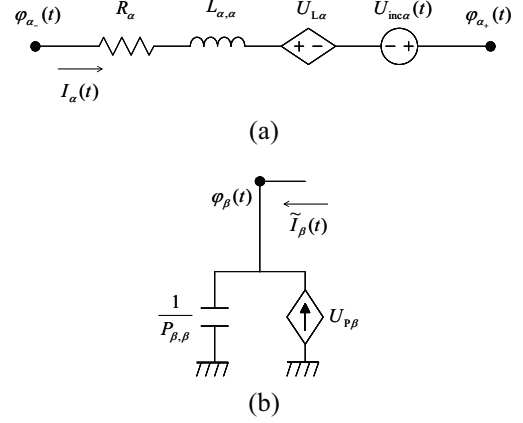

(a)

(b)

Fig. 4. Circuit interpretation of the PEEC. (a) An inductive circuit. (b) A capacitive circuit.

volume cell α

$$R_\alpha I_\alpha(t) + \sum_{a=1}^{N_V} L_{\alpha,a} \frac{\partial I_a(t_{\alpha,a})}{\partial t} + \widetilde{\varphi}_\alpha = U_{\text{inc}\alpha}(t), \; (6)$$

where $U_{\text{inc}\alpha}$ is the incident electromotive force, R_α is the active resistance, and $L_{\alpha,a}$ is the partial inductance between the volume cells α and a. Additionally, $\widetilde{\varphi}_\alpha = \varphi_{\alpha+} - \varphi_{\alpha-}$, where $\varphi_{\alpha+}$ and $\varphi_{\alpha-}$ are the mean values of potentials on the surface cells α_+ and α_- adjacent to the volume cell α, respectively. As a result, the circuit corresponding to the volume cell α is derived as shown in Fig. 4(a). Similarly, from the continuity equation on the surface cell, the circuit associated with the surface cell β can be derived as shown in Fig. 4(b).

In order to derive updating formulas, we apply KVL to the inductive circuit in Fig. 4(a) and KCL to the capacitive circuit in Fig. 4(b). Then, discretizing the KVL and KCL equations in the leapfrog manner leads to the following updating formulas.

$$I_\alpha^{n+1} = \frac{\Delta t R_\alpha - 2L_{\alpha,\alpha}}{\Delta t R_\alpha + 2L_{\alpha,\alpha}} I_\alpha^n$$

$$+ \frac{2\Delta t}{\Delta t R_\alpha + 2L_{\alpha,\alpha}} \left(\widetilde{\varphi}_\alpha^{n+\frac{1}{2}} - U_{\text{L}\alpha}^{n+\frac{1}{2}} + U_{\text{inc}\alpha}^{n+\frac{1}{2}} \right), \; (7)$$

$$\varphi_\beta^{n+\frac{1}{2}} = \varphi_\beta^{n-\frac{1}{2}} + \Delta t P_{\beta,\beta} \left(\widetilde{I}_\beta^n - U_{\text{P}\beta}^n \right). \; (8)$$

Because the controlled sources $U_{\text{L}\alpha}^{n+1/2}$ and $U_{\text{P}\beta}^n$ appear in the right-hand sides of the above equations, the updating formulas are
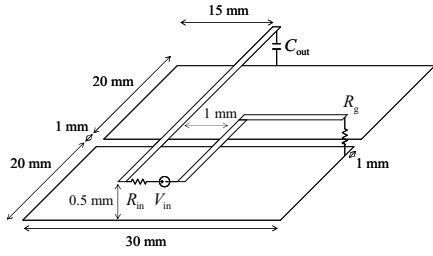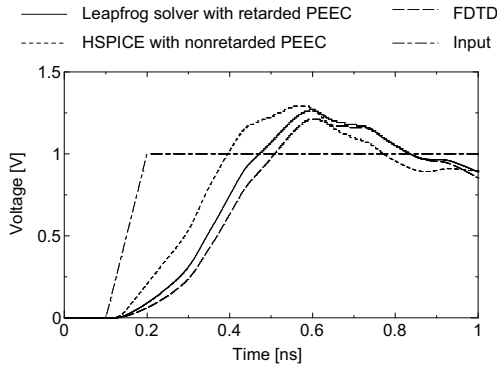
Fig. 5. Example interconnect geometry.

Fig. 6. Waveform results for far end of driving line.

completely explicit: the variables to be updated depend only on the known values. The retarded terms are evaluated by

$$U_{\text{L}\alpha}^{n+\frac{1}{2}} = \sum_{a=1,a\neq\alpha}^{N_Y} \frac{L_{\alpha,a}}{L_{a,a}} \widetilde{U}_{\text{L}a}^{n_{\alpha,a}+\frac{1}{2}} , \qquad (9)$$

$$U_{\text{P}\beta}^{n} = \sum_{b=1,b\neq\beta}^{N_S} \frac{P_{\beta,b}}{P_{\beta,\beta}} \widetilde{I}_{b}^{n_{\beta,b}} , \qquad (10)$$

$$n_{\alpha,a} = n - \left\lfloor \frac{|\mathbf{r}_\alpha - \mathbf{r}_a|}{v\Delta t} \right\rfloor , \qquad (11)$$

and $n_{\beta,b}$ is defined similarly to (11). Thus, we should store *history* of the inductive voltages $\widetilde{U}_{\text{L}a}$ and capacitive currents $\widetilde{I}_b$ during the simulation. For now, we store the past values as many as needed, and do not use an interpolation technique. This is because the time step size used in the simulation is constant and sufficiently small due to a requirement of the numerical stability condition, and adequate accuracy can be achieved even if the approximation (11) is used. In practice, according to the maximum retardation time $T_{d,\max}$ in the simulation, we store at most $\lfloor T_{d,\max} / \Delta t \rfloor$

past values for each controlled source in the KVL and KCL equations. This is implemented by using circular buffers.

We apply the proposed technique to an example structure, which is the interconnect crossing the gap between the two conducting plates as shown in Fig. 5. The waveform results of the branch voltage of the capacitor C_{out} are shown in Fig. 6. In Fig. 6, we can see that the waveform obtained from the proposed method is close to the waveform from the finite-difference time-domain (FDTD) solver whereas the result from HSPICE is different from them. This fact shows that the retardation of the coupling effects should be included for the full-wave simulation. The CPU time taken for the simulation of the leapfrog-based solver is 4.52 s, 15.61 s for HSPICE, and 43.93 s for the FDTD solver. Therefore, the leapfrog scheme is suitable for the full-wave transient simulation based on the PEEC method.

4. Conclusions

In this paper, we have proposed the two types of the transient simulation techniques based on the explicit leapfrog scheme. The numerical results showed that the proposed methods were more efficient than the existing methods in the example simulations.

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Studies of Electrostatic Discharge Simulation

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Abstract

This report describes the recent studies for the simulation techniques of the electrostatic discharge (ESD), which is categorized into two modes, namely contact and air discharge modes. Each of them is based on either circuit or electromagnetic simulation technique. We review some early works and introduce some results.

1. Introduction

Recently, because of the speed-up of operating frequency and lower operating voltage, electronic systems are susceptible to external noises. Especially, the electrostatic discharge (ESD) from an electrically-charged object causes severe problems in the electronic systems. Therefore, the immunity of an electronic equipment to the ESD is becoming more important.

IEC 61000-4-2 is one of the standards for the immunity test of the electronic equipment. In this standard, an ESD generator is usually used to imitate a human-to-metal ESD. We inject the discharge current to an equipment under test (EUT) and evaluate whether the EUT is broken or not.

The waveform of the ESD current is defined as shown in Fig. 1. The standard defines the value of the peak amplitude, rise time, and falling edge of the current. However, these measurement-based immunity tests are considered to be impractical because we can not test frequently in realistic circuit design. Therefore, numerical simulations are necessary to evaluate the immunity to the ESD.

There are two modes of the ESD in the IEC standard, namely contact and air discharge modes. In the test of the contact discharge mode, the electrode of the ESD generator is held in contact with the EUT, and the discharge switch within the generator is actuated to inject the current. As for the air discharge mode, the charged electrode of the generator is brought close to the EUT, and the discharge current flows as a spark to the EUT. It is difficult to reproduce the air discharge in the test even if we use the same approaching speed and charged voltage.

In addition, there are two ways how to simulate the ESD events, namely a circuit and full-wave analyses. The circuit analysis is performed based on the circuit theory and related circuit equations. On the other hand, the full-wave analysis directly deals with the electromagnetic fields governed by Maxwell's equations. This report introduces some of these simulation techniques published in the early works.

2. Contact Discharge Mode

A variety of researches about the simulations of the ESD events in the contact discharge mode have been done. In some of them, the ESD has been interpreted as a current source without any load effect of the ESD generator. However, interactions among the components of the ESD generator such as a metallic tip, a plastic body, and a ground strap affect the current waveform. Therefore, it is necessary to take into account the load effect in the simulation.

In [1], the simulations were performed using both the circuit and the full-wave
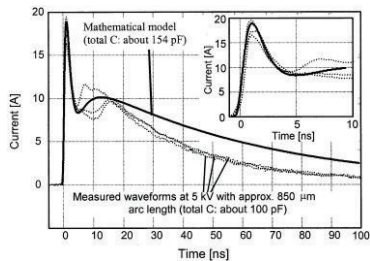
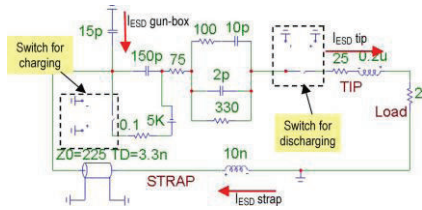Fig. 1. The ESD current waveforms, one of which is defined in the IEC standard.
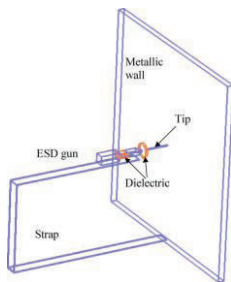

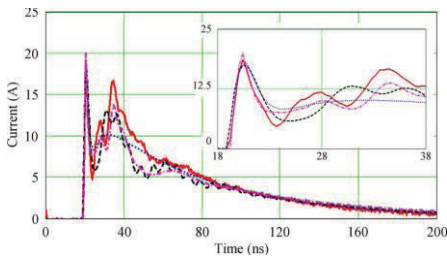Fig. 2. The circuit model in [1].

Fig. 3. The full-wave model in [1].

Fig. 4. The waveform results of the ESD current in [1].

Fig. 5. The ESD current waveforms in [2].

Fig. 6. The magnetic field strength in [2].

Fig. 7. The electric field strength in [2].

models with the load effect. The models used in the simulation are illustrated in Figs. 2 and 3. The circuit model consists of the elements associated with the switches, body, tip, and ground strap connected to the ESD generator. As for the full-wave model, the structures of a metallic wall and ESD generator are directly modeled in the three-dimensional space by a commercially-based simulator.

The waveform results of the ESD currents related to these models are shown in Fig. 4. We can see the good agreements
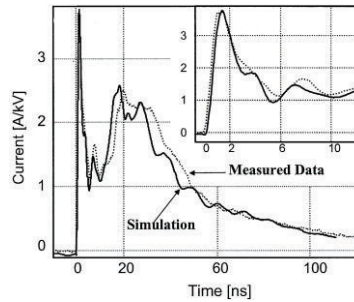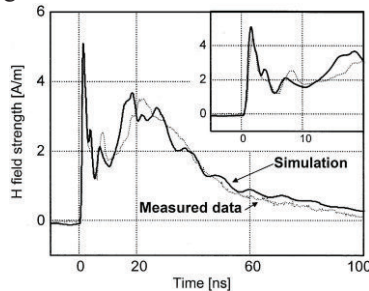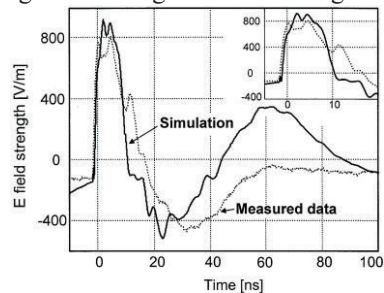
between the results from the measurement, circuit model and full-wave model. Although the circuit model enables to do the fast simulation, it can not calculate the electromagnetic fields distributed over the space. In contrast, the simulation with full-wave model is time-consuming, but it can simulate the radiated electromagnetic fields.

One of the difficulties in the contact discharge mode is modeling the relay, which represents the discharge switch inside the generator. This is because it is necessary to model the switching process of the relay as the time dependent material. However, in general, most of the electromagnetic simulation techniques can not incorporate such a material. In [2], this problem is overcome by developing a full-wave simulator based on the finite-difference
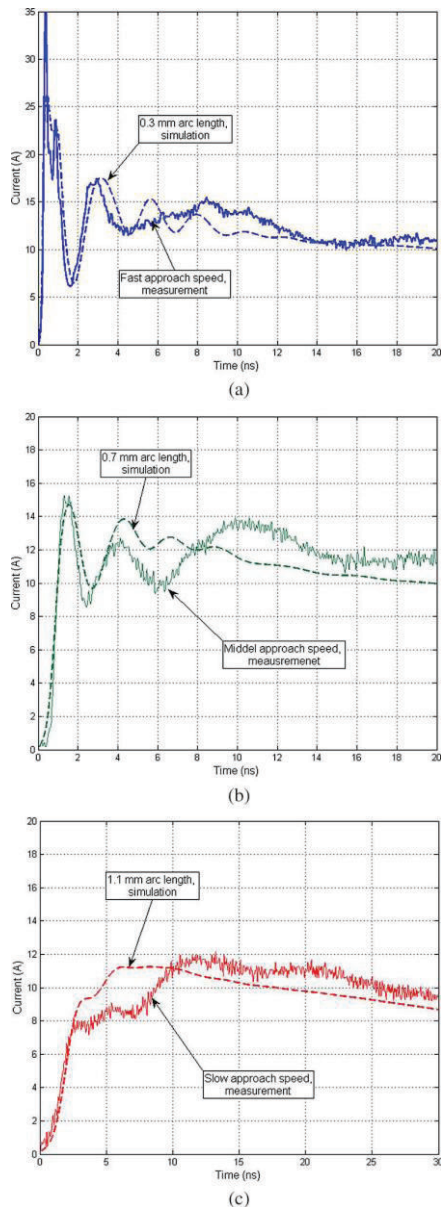
3. Air Discharge Mode

The recent research for the air discharge has been described in [3]. In the air discharge mode, the current waveform depends on an arc length. However, the arc length can not be controlled accurately due to a statistical time lag. In [3], the arc model proposed by Rompe and Weizel has been used to represent the spark. The waveform results are shown in Fig. 8. An agreement can be observed. In the measurement, the arc length is controlled by the approach speed of the ESD generator.

4. Conclusions and Future Works

In this report, we have reviewed the researches for the simulations of the ESD events. I have written the program of the three dimensional FDTD for my graduation thesis. I am now planning to develop a high speed simulator in which the circuit and full wave analyses are combined with each other.

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Fig. 8. The current waveforms related to the arc lengths in [3]. The length used in (b) is the average length between those used in (a) and (c).

time-domain (FDTD) method and incorporating the time dependent material.

The calculated and measured current waveforms at the discharge point are shown in Fig. 5. The magnetic field strength at the distance of 10 cm from the discharge point is shown in Fig. 6. In addition, the electric field strength at the distance of 40 cm from the discharge point is illustrated in Fig. 7. The simulation results in these figures agree well with the measurement results.

Block-Latency Insertion Method for Fast Simulation of Nonlinear Circuit

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Abstract

For the analysis of large network including nonlinear active devices and coupled elements, conventional SPICE-like simulators suffer from a large amount of computational cost due to time-consuming direct matrix operations. In order to overcome the problem, the block-latency insertion method (block-LIM) has been proposed as a fast circuit simulation technique. The advantage of the block-LIM is employing locally matrix solutions. However, there are few applications of the block-LIM to the nonlinear circuit simulation. In this paper, we describe an efficient nonlinear circuit simulation technique by using the nonlinear version of block-LIM, and estimate its characteristics by applying to some example nonlinear circuits.

1. Introduction

Currently, the advancement of the semiconductor packaging technologies has provided the high-speed and high-density electronic circuits. Especially, a low voltage and high-speed signals result in a simultaneous switching noise which induces significant signal/power integrity problems [1]. In order to estimate these effects accurately, the equivalent circuit, including the large scale linear passive network and the nonlinear active one illustrated in Fig. 1, has to be analysed [2]. Thus, conventional SPICE-like simulators take an enormous amount of time for the simulation of such a circuit. Therefore, some kind or another fast circuit simulation method is strongly needed.

Recently, several kinds of fast circuit simulation techniques for nonlinear networks have been proposed [2], [3]. The LIM is one of them, and based on a leapfrog algorithm. In the LIM, it is assumed that the circuit to be analysed is composed of branch topologies and node topologies. In addition, each topology in the circuit must contain a reactance element: if there exists a branch without inductance or a node without shunt
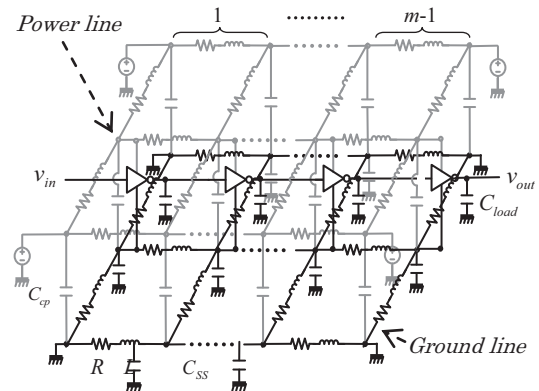

Fig. 1. Equivalent circuit of distribution network with nonlinear element

capacitance, a small inductance or shunt capacitance is inserted into those topologies. By this treatment, an arbitrary circuit can be completely represented by using branch and node topologies. In order to generate updating formulas of the LIM, the Kirchhoff's voltage low (KVL) and the Kirchhoff's current low (KCL) are applied to the branch topology and the node topology, respectively. Then, the leapfrog algorithm is used for the solutions of the KVL and KCL equations, where the unknown variables can be updated by using explicit substitutions without using the direct method.

On the other hand, since the LIM is based on the explicit finite difference method, it has a limitation of a time step size to satisfy the numerical stability condition. Concretely, the maximum time step size of the LIM, Δt_{max}, has the following upper bound:

$$\Delta t_{max} < \sqrt{2} \min_{j=1}^{N_n} \left(\sqrt{\frac{C_j}{N_b^j} \min_{m=1}^{N_b^j} \left(L_{jm} \right)} \right), \quad (1)$$

where N_n is the total number of nodes in the circuit, N_b^j is the number of the branches connected to the node j, L_{jm} is a value of the inductor in the branch connected to the node j, and C_j is a value of the grounded capacitor connected to the node j.

By extending the basic LIM algorithm, the block-LIM [4] has been proposed for a fast multiconductor transmission lines analysis. In this paper, we propose an efficient nonlinear circuit simulation technique based on the block-LIM algorithm.

2. Block-Latency Insertion Method

The block-LIM regards the topologies connected by mutual inductance and mutual capacitance as block topologies as shown in Fig. 2. Additionally, the block-LIM assumes that the circuit is composed of the basic branch and node topologies, and the branch block and node block topologies, and the variables in these topologies are updated by applying the leapfrog algorithm.

In order to generate the updating formulas of the block-LIM, the KVL and the KCL are applied to the basic/block node and branch topologies in the circuit, respectively. These KVL and KCL equations can be written simultaneously in a vector-matrix form:

$$\begin{bmatrix} \mathbf{G} & \mathbf{M} \\ -\mathbf{M}^T & \mathbf{R} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \mathbf{C} & \mathbf{0} \\ \mathbf{0} & \mathbf{L} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{v} \\ \mathbf{i} \end{bmatrix} = \begin{bmatrix} \mathbf{h} \\ \mathbf{e} \end{bmatrix}, \quad (2)$$

where $\mathbf{v}$, $\mathbf{i}$, $\mathbf{h}$, and $\mathbf{e}$ are a node voltage vector, a branch current vector, an independent current source vector, an independent voltage source vector, respectively. In addition, $\mathbf{R}$, $\mathbf{L}$, $\mathbf{C}$, and $\mathbf{G}$ are a resistance matrix, an inductance matrix, a capacitance matrix, and a conductance matrix, respectively. And $\mathbf{M}$ is an incidence matrix which represents of the connection of the topologies. The dimensions of the vectors and sub-matrices in (2) are defined as
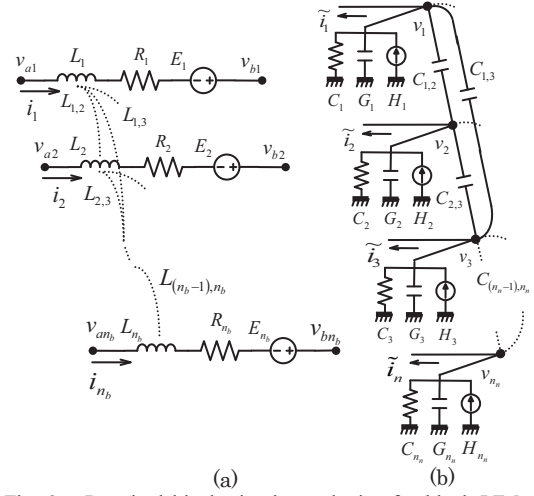

(a)　　　　　　(b)

Fig. 2. Required block circuit topologies for block-LIM. (a) Branch block topology. (b) Node block topology.

$\mathbf{v}$, $\mathbf{h} \in \Re^{N_n}$, $\mathbf{i}$, $\mathbf{e} \in \Re^{N_b}$,
$\mathbf{R}$, $\mathbf{L} \in \Re^{N_b \times N_b}$, $\mathbf{C}$, $\mathbf{G} \in \Re^{N_n \times N_n}$, $\mathbf{M} \in \Re^{N_n \times N_b}$.
Then, applying the difference method based on the leapfrog algorithm to (2) leads to

$$\begin{bmatrix} \frac{1}{\Delta t}\mathbf{C}+\mathbf{G} & \mathbf{0} \\ -\mathbf{M}^T & \frac{1}{\Delta t}\mathbf{L} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{v}^{n+\frac{1}{2}} \\ \mathbf{i}^{n+1} \end{bmatrix} = \begin{bmatrix} \frac{1}{\Delta t}\mathbf{C}+\mathbf{G} & -\mathbf{M} \\ \mathbf{0} & \frac{1}{\Delta t}\mathbf{L} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{v}^{n-\frac{1}{2}} \\ \mathbf{i}^{n} \end{bmatrix} + \begin{bmatrix} \mathbf{h}^{n} \\ \mathbf{e}^{n+\frac{1}{2}} \end{bmatrix}, (3)$$

where n and Δt are a time index and the timestep size, respectively. Note that the coefficient matrix of the left-hand side of (2) is a lower block triangular matrix, current and voltage variables can be solved independently.

3. Nonlinear Block-LIM

The LIM [3] can treat only two-terminal nonlinear elements. This is because the KCL equations at the nodes which are connected to more than two-terminal nonlinear elements are represented as simultaneous equations. Therefore, the node voltages are not solved individually.

We generate the updating formula of the proposed method below, using MOSFET as an example of the nonlinear element. In Fig. 3, CMOS inverter which is composed of PMOS and NMOS is shown as an example in which some nodes are connected to the power and the ground lines by parasitic capacitances. Furthermore, a nonlinear block consists of a set of nodes, out, DD, and SS. Applying the KCL to each node in the nonlinear block topology leads to the

following simultaneous equations in a vector-matrix from

$$\frac{d}{dt}\begin{bmatrix} C_{load} & 0 & 0 \\ 0 & C_{cp} & -C_{cp} \\ 0 & -C_{cp} & C_{cp}+C_{SS} \end{bmatrix} \cdot \begin{bmatrix} v_{out} \\ v_{DD} \\ v_{SS} \end{bmatrix} + \begin{bmatrix} i_{Dp}+i_{Dn} \\ -i_{Dp} \\ -i_{Dn} \end{bmatrix} + \begin{bmatrix} i_{out} \\ \tilde{i}_{DD} \\ \tilde{i}_{SS} \end{bmatrix} = \mathbf{0}, \quad (7)$$

where i_{Dp} and i_{Dn} are the drain currents flowing through PMOS and NMOS, respectively, and $\tilde{i}_{DD}$ and $\tilde{i}_{SS}$ are the sum of currents flowing out the nodes DD and SS respectively. Then, applying the difference method based on the leapfrog algorithm to (7) leads to

$$\frac{1}{\Delta t}\begin{bmatrix} C_{load} & 0 & 0 \\ 0 & C_{cp} & -C_{cp} \\ 0 & -C_{cp} & C_{cp}+C_{SS} \end{bmatrix} \cdot \begin{bmatrix} v_{out}^{n+\frac{1}{2}}-v_{out}^{n-\frac{1}{2}} \\ v_{DD}^{n+\frac{1}{2}}-v_{DD}^{n-\frac{1}{2}} \\ v_{SS}^{n+\frac{1}{2}}-v_{SS}^{n-\frac{1}{2}} \end{bmatrix} + \begin{bmatrix} i_{Dp}^{n+\frac{1}{2}}+i_{Dn}^{n+\frac{1}{2}} \\ -i_{Dp}^{n+\frac{1}{2}} \\ -i_{Dn}^{n+\frac{1}{2}} \end{bmatrix} + \begin{bmatrix} i_{out}^{n} \\ \tilde{i}_{DD}^{n} \\ \tilde{i}_{SS}^{n} \end{bmatrix} = \mathbf{0}, \quad (8)$$

Note that the second term of the left hand side in (8) is a nonlinear function vector. Thus, the proposed method exploits the Newton-Raphson (NR) method to solve (8) defining the left hand side of (8) as a nonlinear function vector $\mathbf{f} = [f_1 \quad f_2 \quad f_3]^{\mathrm{T}}$, and applying the NR method to $\mathbf{f}$ leads the following updating formula of the nonlinear block topology:

$$\mathbf{j}\left(\mathbf{v}^{n+\frac{1}{2},(k-1)}\right) \cdot \mathbf{v}^{n+\frac{1}{2},(k)} = \mathbf{j}\left(\mathbf{v}^{n+\frac{1}{2},(k-1)}\right) \cdot \mathbf{v}^{n+\frac{1}{2},(k-1)} - \mathbf{f}^{(k-1)}, \quad (9)$$

where

$$\mathbf{j}\left(\mathbf{v}^{n+\frac{1}{2},(k-1)}\right) = \begin{bmatrix} \dfrac{\partial f_1^{(k-1)}}{\partial v_{out}^{n+1/2,(k-1)}} & \dfrac{\partial f_1^{(k-1)}}{\partial v_{DD}^{n+1/2,(k-1)}} & 0 \\[2mm] \dfrac{\partial f_2^{(k-1)}}{\partial v_{out}^{n+1/2,(k-1)}} & \dfrac{\partial f_2^{(k-1)}}{\partial v_{DD}^{n+1/2,(k-1)}} & \dfrac{\partial f_2^{(k-1)}}{\partial v_{SS}^{n+1/2,(k-1)}} \\[2mm] 0 & \dfrac{\partial f_3^{(k-1)}}{\partial v_{DD}^{n+1/2,(k-1)}} & \dfrac{\partial f_3^{(k-1)}}{\partial v_{SS}^{n+1/2,(k-1)}} \end{bmatrix},$$

$$\mathbf{v}^{n+\frac{1}{2},(k)} = \begin{bmatrix} v_{out}^{n+\frac{1}{2},(k)} & v_{DD}^{n+\frac{1}{2},(k)} & v_{SS}^{n+\frac{1}{2},(k)} \end{bmatrix}^{\mathrm{T}},$$

$$\mathbf{f}^{(k-1)} = \begin{bmatrix} f_1^{(k)} & f_2^{(k)1} & f_3^{(-k)} \end{bmatrix}^{\mathrm{T}}$$

and k is an iteration count of the NR method. The unknown variables in the nonlinear block topology are updated by solving (9) iteratively until the iterative solutions converge. Moreover, this algorithm can be easily applied to the nonlinear device with more than two-terminals by changing the size of the matrices and vectors in (9).

Fig. 4 shows a graphical representation of the unknown variables of (3) in the case that the proposed method is applied to the circuit shown in Fig. 1. Note that the coefficient matrices of the nonlinear block topology,
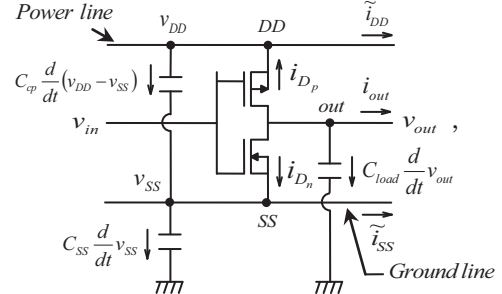

Fig. 3. Enlarged part of nonlinear circuit with CMOS inverter in Fig. 1.

which is composed of the nodes connected to the CMOS inverters, is a 3×3 local dense matrix. Additionally, the coefficient matrix of the linear block topology, which is composed of the nodes connected to each mutual capacitance, is a 2×2 local dense matrix. In the proposed method, the nonlinear node block topology is updated by using (9) while the linear node block and branch topologies are updated based on the basic block-LIM algorithm. Thus, the nonlinear block-LIM does not require the matrix operation for the whole system similarly to the block-LIM. In addition to the above advantage, the proposed method can reduce the number of fill-ins caused by the LU factorization. Fig. 5 shows the coefficient matrix with fill-ins after the LU factorization. Note that the matrix in Fig.5 contains a number of non-zero entries even though the original coefficient matrix is sparse. On the other hand, the proposed method inhibits the fill-ins because this method performs the direct matrix operations and the calculations of the Jacobian matrix only within the block topology. Hence, the proposed method can reduce the computational costs significantly compared with SPICE-like simulators.

4. Numerical Results

In order to estimate the validity and efficiently of the proposed method, we analyze an example network by using the proposed method and the HSPICE. The network is composed of power and ground lines with m CMOS inverters between these lines as shown in Fig. 1. The element values are $R = 0.1\Omega$, $L = 0.1$ μH, $C_{load} = 0.1$ pF, $C_{cp} = 1.0$ fF, and $C_{SS} = 0.1$pF, and the parameters

TABLE I

Parameter	PMOS	NMOS	Unit
$K_{p,n}$	8.362	20.072	μA/V^2
$W_{p,n}$	2.0	2.0	μm
$L_{p,n}$	1.0	1.0	μm
$V_{Tp,Tn}$	-0.134	0.134	V
$\lambda_{p,n}$	0	0	V^{-1}

TABLE II

Element	n	HSPICE [s]	Proposed method [s]	Speed-up ratio
139	5	4.70	0.69	6.8
284	10	9.33	0.88	10.6
574	20	20.40	1.41	14.5
1444	50	54.54	2.77	19.7
2894	100	110.02	5.32	20.7

used in all of MOSFETs are shown in TABLE I. In this case, the time step size derived from (1) is equal to 7.72 ps. The input voltage is trapezoidal pulse of which an initial value is 0 V, a pulse value is 3.3 V, a delay time is 0 ns, a rise and fall time are 10 ns, a pulse width is 40 ns, and a period is 100 ns, is connected to the first CMOS inverter. The simulation interval is from 0 ns to 500 ns. The voltage waveforms observed at the 100th CMOS inverter is shown in Fig. 6. It is confirmed that the waveform from the proposed method agrees with that of the HSPICE. TABLE II shows the CPU times and speedup ratio on the basis of the CPU time of the HSPICE in case of changing m from 5 to 100. In TABLE II, it can be seen that speed-up ratio is increasing as m is doing. As a result, we have confirmed that the proposed method is more appropriate for the large nonlinear network analyses than the conventional SPICE-like simulators.

5. Conclusions

In this paper, the fast circuit simulation technique based on the block-LIM algorithm for the large linear network with nonlinear devices has been described. The proposed method regards the nodes, which are connected each other by nonlinear device, as one nonlinear block topology. The proposed method can perform the fast circuit analysis because the method has two superior features compared with SPICE-like simulators: that is to say, the local matrix operations, and the reduction of fill-ins in the LU factorization.
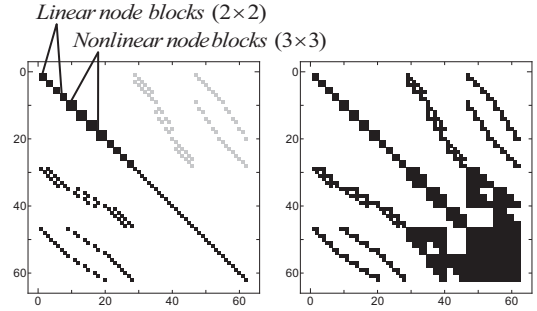

Fig. 4. Graphical representation of the coefficient matrix in proposed method.

Fig. 5. Graphical represent-tation of the coefficient matrix inSPICE-like simul-ators after LU factorization.
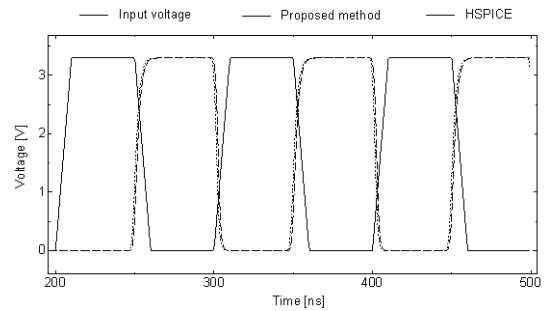

Fig. 6. Waveform results

Some numerical results have shown that the proposed method is about 20 times faster than the HSPICE with appropriate accurancy.

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Eye-diagram of a High-speed Through Silicon Via Channel

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Abstract

An eye-diagram estimation method for a through-silicon via (TSV) based three-dimensional integrated circuit (3D IC) was developed. To validate the proposed method, circuit-level simulations and time-domain measurements of a fabricated 3D IC test vehicle were performed at different data rates. The eye-diagrams estimated by the proposed method had good correlations with those of the circuit-level simulations and time-domain measurements.

I. INTRODUCTION

Spurred by industrial demand for integrated-circuit systems with improved channel bandwidths and compact sizes, three-dimensional integrated circuit (3D IC) technology is a potential solution [1]. 3D IC realizes vertical interconnections between heterogeneous chips and provides impressively short channel paths. Through silicon via (TSV) and silicon interposer are used to achieve shorter channel lengths and are the most important technologies in 3D IC. However, as shown in Fig. 1, although the channel length can be reduced by TSV and interposer, signal integrity still cannot be ensured in 3D IC as the data rate increases.
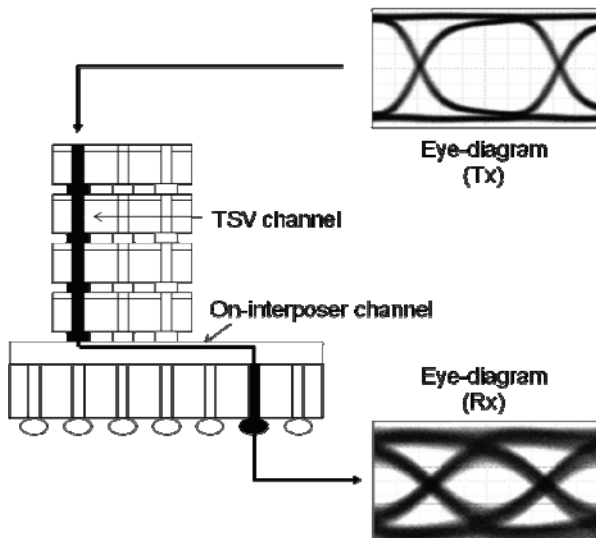

Figure 1. Eye-diagram degradation in 3D IC channel

The eye-diagram, which is a convenient graphical method used to analyze the received digital signal, is widely used to analyze signal integrity. However, to obtain the eye-diagram of 3D IC channel is difficult because of the complexity of the channel. Simulation and measurement of the eye-diagram in TSV-based 3D IC have several limitations: for example, they are time consuming and require the fabrications of test vehicles. Though there have been the previous studies that efficiently estimate the eye-diagrams, these methods have the limited accuracy in 3D IC because their target channels are too simple [2-3]. Therefore, the method to efficiently estimate the precise eye-diagram of TSV-based 3D IC channels is needed.

In this paper, we propose an efficient eye-diagram estimation method for TSV-based 3D IC. Because the proposed method employs the worst-case data patterns as the input instead of a Pseudo Random Bit Sequence (PRBS), the eye-diagram of the TSV-based 3D IC channel can be estimated quickly. Moreover, to estimate the precise eye-diagram in TSV-based 3D IC channel, the proposed method employs the mathematical models of the multi-stacked TSV and the silicon interposer interconnect. By using the developed models, the precise eye-diagram of TSV-based 3D IC channel can be estimated.

To verify the proposed eye-diagram estimation method for TSV based 3D IC, test vehicle consisting of TSV and silicon interposer was fabricated. As a result of the time-domain measurement of the test vehicle with various data rates, the eye-diagrams estimated by the proposed method correlates well with the measurement results; the maximum error rates of eye-opening voltage and timing jitter were 7.0% of peak-to-peak voltage (V_{p-p}) and 9.0% of 1 unit interval (UI), respectively. Moreover, the proposed method was also compared to circuit-level simulation, and eye-diagrams estimated by the proposed method and simulation were almost same.

II. EYE DIAGRAM ESTIMATION METHOD FOR A TSV-BASED 3D IC CHANNEL

A. ABCD matrix of 3D IC channel

Many poles and zeros exist in real channels; thus, predicting the voltage-transfer function of the channel by considering all poles and zeros is almost impossible. Therefore, we used an equivalent-circuit model of the channel consisting of the dominant poles and zeros instead. For the TSV-based 3D IC channel, we employ equivalent-circuit models of TSV and silicon interposer interconnect; previous studies for equivalent-circuit models of them can be found elsewhere [4-5].

Using the equivalent-circuit models, the ABCD matrices of the multi-stacked TSV channel and the silicon interposer interconnect can be obtained as shown in (1) and (2), respectively; the channel is assumed to one-layer ground-signal-ground (GSG) type. The symbol descriptions are shown in Table 1. For the silicon interposer, the ABCD matrix includes the exponent, M, which accounts for the long interconnect length; the equivalent-circuit model of a long interconnect should be the distributed model. If we have the ABCD matrices of Tx and Rx drivers, the ABCD matrix of a TSV-based 3D IC channel can be derived by combining them with (1) and (2). The voltage-transfer function of a TSV-based 3D IC channel can be obtained from the matrix [6].

$$\begin{bmatrix} A_{TSV} & B_{TSV} \\ C_{TSV} & D_{TSV} \end{bmatrix}$$

$$\approx \begin{bmatrix} 1 + N^2\left(R_{TSV} + sL_{TSV}\right) \times \left(\dfrac{2.4 \times sC_{ox}(G_{Si} + sC_{si})}{G_{si} + s(1.2C_{ox} + C_{si})}\right) & N\left(R_{TSV} + sL_{TSV}\right) \\ N\left(\dfrac{2.4 \times sC_{ox}(G_{Si} + sC_{si})}{G_{si} + s(1.2C_{ox} + C_{si})}\right) & 1 \end{bmatrix} \quad (1)$$

where N = the number of stacked TSV

$$\begin{bmatrix} A_{Int} & B_{Int} \\ C_{Int} & D_{Int} \end{bmatrix}$$

$$\approx \begin{bmatrix} 1 + \left(R_{Int} + sL_{Int}\right) \times \left(sC_{Pass} + \dfrac{\frac{2}{3}sC_{oxide}\left(G_{silicon} + sC_{silicon}\right)}{G_{silicon} + s\left(\frac{2}{3}C_{oxide} + C_{silicon}\right)}\right) & R_{Int} + sL_{Int} \\ sC_{Pass} + \dfrac{\frac{2}{3}sC_{oxide}\left(G_{silicon} + sC_{silicon}\right)}{G_{silicon} + s\left(\frac{2}{3}C_{oxide} + C_{silicon}\right)} & 1 \end{bmatrix}^{M} \quad (2)$$

TABLE I. DESCRIPTION OF SYMBOLS IN (1) AND (2)

Symbol	Description
$R_{TSV/}$	Resistance of TSV and bump
L_{TSV}	Inductance of TSV and bump
C_{ox}	Capacitance of oxide layer in TSV
C_{Si}	Capacitance of silicon substrate between TSVs
G_{Si}	Conductance of silicon substrate between TSVs
R_{Int}	Resistance of interposer interconnect
L_{Int}	Inductance of interposer interconnect
C_{oxide}	Capacitance of oxide layer under metal line
C_{pass}	Fringing capacitance of passivation layer
$C_{silicon}$	Fringing capacitance in silicon substrate
$G_{silicon}$	Conductance of silicon substrate

B. Eye diagram estimation method

A summary of the flow of the proposed eye-diagram estimation method is shown in Fig. 2.
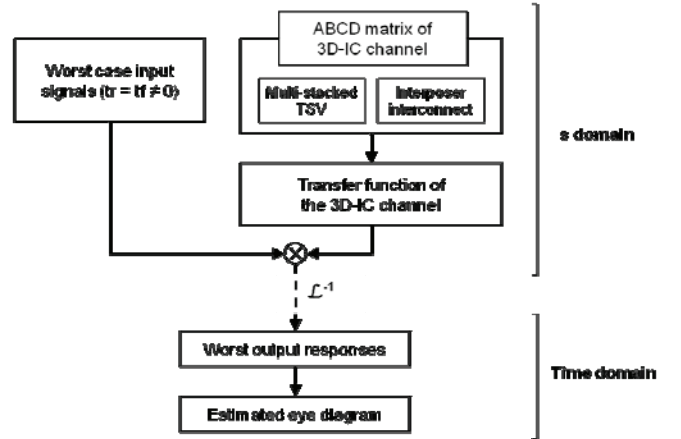

Figure 2. Flow chart for the eye-diagram estimation method

In the first step, we define the worst case input signals in the s domain. If we neglect the effect of reflection, we can assume a unit pulse signal with non-zero rising and falling times as the worst-case input signal that corresponds to the worst output response. In subsequent steps, the proposed method estimate the eye-diagram by combining the defined worst input signals and the derived voltage transfer function. By multiplying the input by the voltage transfer function, the output response in the s domain can be obtained, and the *inverse Laplace transform* of this response becomes the worst output response in time-domain. Because the inner contour of the eye-diagram, which is the performance metric of signal integrity, is determined by the worst output responses, we can estimate the eye-diagram of TSV-based 3D IC channel.

III. VERIFICATION OF EYE-DIAGRAM ESTIMATION METHOD BY SIMULATION AND MEASUREMENT

To verify the proposed eye-diagram estimation method, the test vehicle of the TSV-based 3D IC that are composed of TSV and silicon interposer was fabricated. Fig. 3(a), (b) and (c) respectively show the cross-section, top and bottom views of the test vehicle, which consists

of two TSVs and a short interposer interconnect; Fig. 3(a) was obtained from the scanning electron microscope (SEM) image. Two chips were stacked vertically, and the TSV channel and interposer interconnect were fabricated on the top and bottom chips, respectively. Because of the short length of the interposer interconnect (=500 μm) and large amount of C_{ox} which came from large TSV diameter (=46 μm) and thin thickness of the oxide-layer in TSV (=0.5 μm), the TSVs had the considerable channel loss.

For the time-domain measurement, a digital sampling oscilloscope, TDS8000B from Tektronix with a bandwidth of 20 GHz was used. The input signal was generated by a pulse pattern generator (PPG), MP-1763C from Anritz, with rise and fall times of 30 ps, and a PRBS of $2^{11}-1$ was used for the input data patterns. The high-frequency cables with a maximum frequency of 40 GHz were used to minimize the effect of cable loss to the measured eye-diagram.

(a)

(b)

(c)
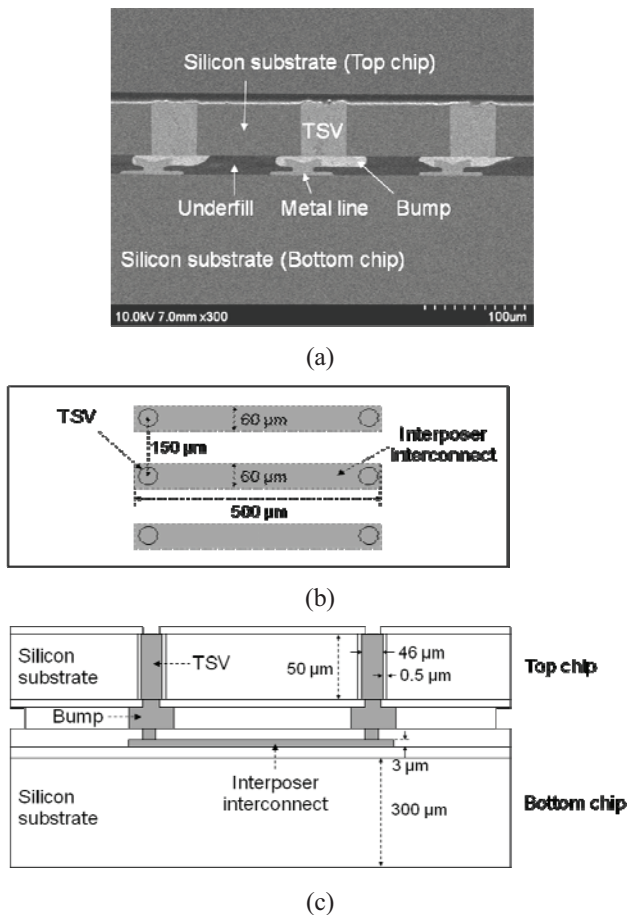
Figure 3. Fabricated test vehicle for measuring the eye-diagram of TSV-based 3D IC channel (a) cross-section view and (b) top view and (c) side view

Fig. 4(a) and (b) respectively, show the estimated and measured eye-diagrams at a data rate of 10 Gbps. The proposed method successfully estimated the almost same eye-diagram with that of time-domain measurement. The error rates of the eye-opening voltage (V_{EOV}) and timing jitter (t_{TJ}) were 7.0% of V_{p-p} and 9.0% of 1 UI, respectively.

There are several factors that contribute to errors: the loss of cables, ringing of the input signal in PPG and random jitters (RJ). Though the eye-diagrams estimated by the proposed method only considered the channel loss of the test vehicle, the measured eye-diagrams additionally contained the loss of the high-frequency cables; it made the measured eye-diagrams degraded more. Moreover, because there was ringing in the input signal of the PPG when we measured the eye-diagram, the shape of the measured eye-diagram is distorted. Though the effect of the ringing was negligible at the low data rate as shown in Fig. 4(b), it became considerable at the high data rate because of the reduced duty-cycle as shown in Fig. 5(b). In addition, though there must be RJ in the measured eye-diagram, the proposed method takes into account data-dependent jitter (DDJ) only. It also made the measured eye-diagram worse than the eye-diagram estimated by the proposed method.
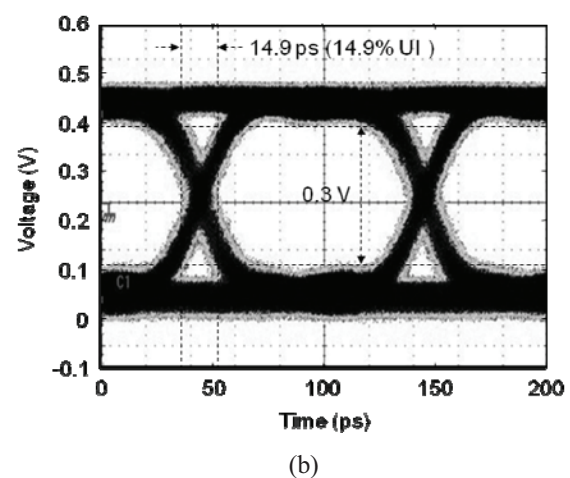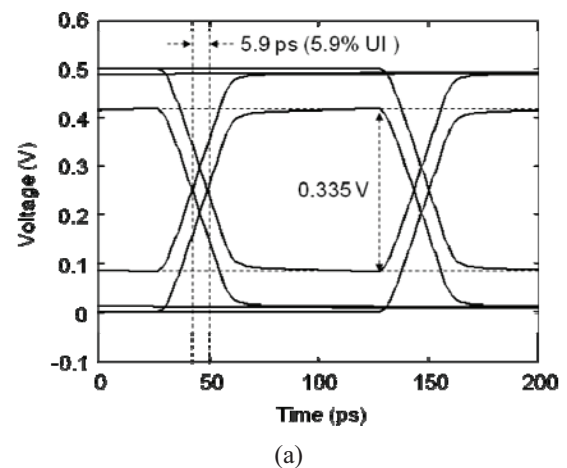

(a)

(b)

Figure 4. Eye-diagrams of TSV-based 3D IC channel in test vehicle at a data rate of 1 Gbps (a) using the proposed method and (b) measurement

Fig. 5(a) and (b) respectively depict V_{EOV} and t_{TJ} in accordance with the data rates. They were obtained by the proposed method, circuit-level simulation and time-domain measurement. *Agilent ADS 2008* was used for the simulator to estimate the eye-diagram by using the equivalent-circuit model of TSV-based 3D IC channel. V_{EOV} and t_{TJ} of simulation results that neglected the cable loss were almost same with those of the proposed method; the maximum error rates of V_{EOV} and t_{TJ} were 4.0% of V_{p-p} and 1.9% of 1 UI, respectively. However, the measured eye-diagrams were worse than the eye-diagrams estimated by the proposed method and circuit-level simulation because of the aforementioned error factors; compared to the proposed method, the maximum error rates of V_{EOV} and t_{TJ} were 7.0% of V_{p-p} and 9.0% of 1 UI, respectively. For the circuit-level simulation including the cable loss, the amount of V_{EOV} and t_{TJ} became close to those of the measurement. Therefore, if we have the ABCD matrix of the cable, the proposed method would be able to estimate the more accurate eye-diagram by considering the cable loss.
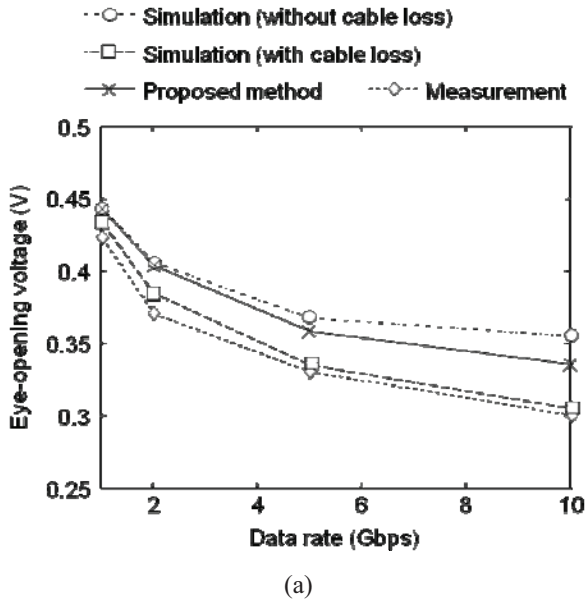

(b)
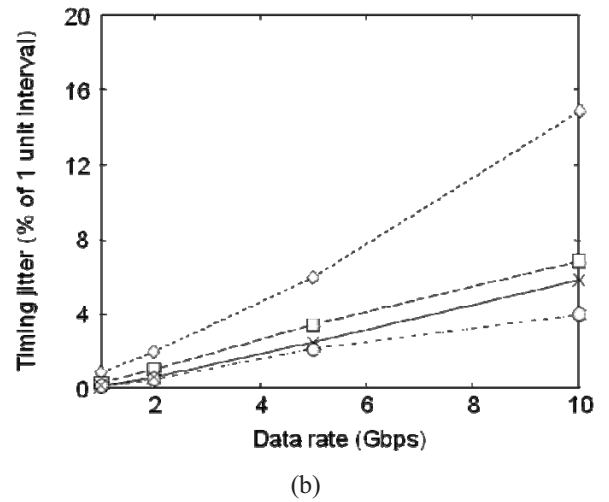
Figure 5. (a) Eye-opening voltages and (b) timing jitters of TSV-based 3D IC channel in test vehicle in accordance with data rate

IV. CONCLUSIONS

In this study, a method to estimate the precise eye-diagram of high-speed channel in a TSV-based 3D IC was proposed. Equations for the ABCD matrices of the multi-stacked TSV and the silicon interposer interconnect were developed to model the eye-diagram of the TSV-based 3D IC chanel. To verify the proposed method, a test vehicle of TSV-based 3D IC was fabricated and the eye-diagrams were estimated, simulated and measured with various data rates. Compared to the circuit-level simulation, the proposed method estimated the eye-diagram within error rates of 4.0% of V_{p-p} and 1.9% of 1 UI in V_{EOV} and t_{TJ}, respectively. Moreover, it was successfully demonstrated that the proposed method can predict the measured eye-diagram of TSV-based 3D IC channel within error rates of 7.0% of V_{p-p} and 9.0% of 1 UI in V_{EOV} and t_{TJ}, respectively.

(a)

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Through-Silicon Via (TSV) Depletion Effect

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Abstract

The effects of through-silicon via (TSV) depletion are analyzed based on the frequency- and time-domain measurements in this paper. As TSV dc bias voltage increases, a TSV depletion region is generated; this region decreases TSV noise coupling at frequencies below 1 GHz. It also creates duty-cycle distortion of the coupled signal, which results from the nonlinearity of the TSV.

1. Introduction

TSV is constructed from conductive via, silicon, and an insulation layer between the via and the silicon; it constructs metal-insulator-silicon (MIS) junction as shown in Fig. 1. Accumulation, depletion, and inversion modes occur in such MIS structures based on the bias voltage between metal and silicon [1]-[2].

In this paper, TSV depletion effects on TSV noise coupling are analyzed using frequency- and time-domain measurements. The test vehicles are manufactured by Hynix semiconductor Inc. using via-last TSV. Even though TSV depletion may occur at all frequencies, the effects of TSV coupling are limited to frequencies below 1 GHz, where TSV capacitance plays a major role in the coupling. As the TSV dc bias voltage increases, the TSV coupling capacitance decreases, which also decreases TSV noise coupling. Unlike small signal

Fig. 1. The conceptual structures and simplified equivalent circuit model of TSV in the depletion mode.

analysis in the frequency domain, large signal analysis in time domain is not simple. For large signals, the bias voltage cannot be considered a fixed value; it changes over time. The bias voltage generates nonlinear voltage-dependent TSV depletion capacitance and creates duty-cycle distortion in the coupling voltage measurements.

2. ANALYSIS OF TSV DEPLETION EFFECT FOR SMALL SIGNALS

To analyze the TSV depletion effect, the noise transfer function between the TSV and substrate contact is measured with varying TSV dc bias voltage. The test vehicle is manufactured by Hynix semiconductor Inc. by using via-last TSV. It contains one TSV, one substrate contact, a common ground for the reference, and probing pads. The diameter of the TSV is 33 um, the size of the substrate contact is 30 um × 30 um, and the distance between the TSV and substrate contact is 100 um. More detailed dimensions of the test vehicle are described in a previous paper and are omitted in this paper [3].

The measured noise transfer function with TSV dc bias voltage variation is shown in Fig. 2. As the dc bias voltage decreases from +3 V to -3 V, the noise transfer function increases from -46.7 dB to -41.7 dB at 10 MHz, while the high-frequency behavior remains same. At low frequencies, TSV coupling is mainly determined by TSV capacitance, CTSV, while mid and high
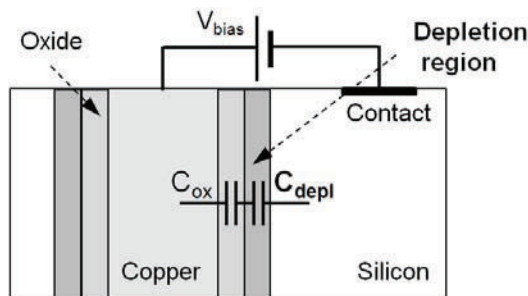
frequency coupling is determined by silicon resistance and capacitance [3].
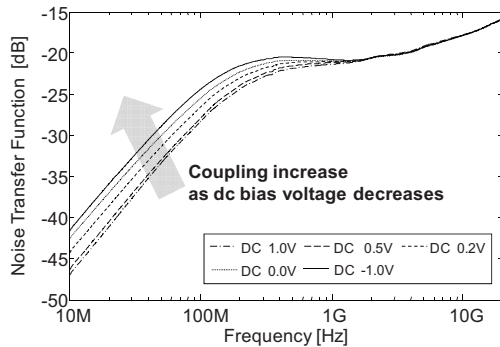

Fig. 2. Noise transfer function (S21) differences depending on TSV dc bias voltage

3. ANALYSIS OF TSV DEPLETION EFFECT FOR LARGE SIGNALS

In this chapter, large signal analysis is performed based on the measurements using signal generator, oscilloscope, and spectrum analyzer. The original injected signal and the coupled signal with 0V TSV dc bias is compared in Fig. 3. We can easily recognize that the duty-cycle distortion occurs at the coupled signal even though there's no duty-cycle distortion at the original signal.
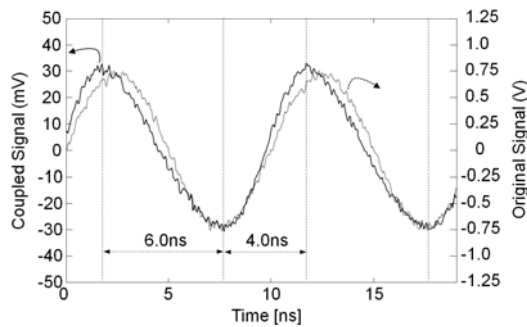
Fig. 3. Duty-cycle distortion of the coupled signal when TSV dc bias voltage is 0V. 100MHz, 750mV amplitude sinusoidal wave is injected to TSV

Fig. 4 illustrates the measured frequency spectrum of the original and the coupled signal when dc bias voltage is 0 V and -3 V. for the harmonic frequencies, there exists some strange phenomena. For DC 0V case at 200MHz, the difference between the original and the coupled signal is very small, which cannot be explained by the noise transfer function. For 400MHz, 500MHz, and 600MHz, the injected input signal has the

power under noise floor while the coupled signal has much larger power than the input signal. It means that the harmonic components are generated during the TSV coupling. At dc -3V, there's small capacitance variation for the large dc voltage variation while it has large variation at dc 0V. This is the reason of much smaller nonlinearity of dc -3V case.
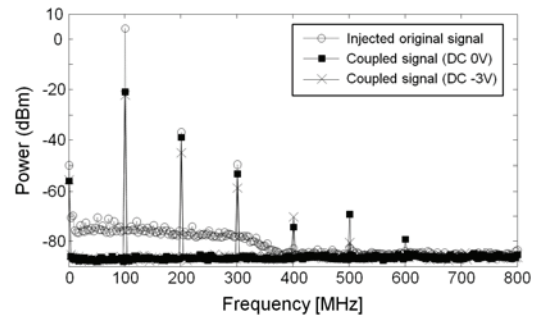

Fig. 4. Measured frequency spectrum of the injected original signal and the coupled signal. The sinusoidal signal with 100MHz frequency and 750mV amplitude is mixed with TSV dc voltage and injected into TSV.

4. Conclusion

The analysis, measurements using a TSV coupling test vehicle are performed. The TSV capacitance decreases as the dc bias voltage increases for the small signal in the depletion mode. For the large signal that varies between VFB and VTh, the results indicated nonlinearity in the time-domain measurements because the TSV capacitance changes with time. This results can be applied to not only TSV coupling but also the TSV channel and other TSV applications.

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I/O Power Estimation and Analysis of High-speed Channels in Through-Silicon Via (TSV)-based 3D IC

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Abstract

In this paper, power estimations for various through-silicon via (TSV)-based three-dimensional integrated circuit (3D IC) designs were conducted in efforts to realize low-power-consumption 3D IC. In addition, the dominant power-consuming factor was found among the TSV-based interconnect components by a power comparison analysis based on the proposed model.

1. Introduction

Recently, through-silicon via (TSV)-based three-dimensional integrated circuits (3D IC) are the leading technology for smaller form factor and higher system performance. With the reduced interconnection length by using a TSV as a vertical interconnection method between stacked dies, the TSV-based 3D IC has become the key solution to reducing power consumption. In this study, we estimated the power dissipation of the TSV-based I/O channel in a 3D IC. As shown in Figure 1, there are two main factors to be considered in power management of a TSV-based I/O channel in a 3D IC: the TSV-based interconnect and the I/O circuitry. Because the I/O driver must be optimized by considering the channel characteristics and signal integrity issues such as reflection, termination, etc., the dynamic and leakage power consumptions due to the I/O driver were not considered in this work. Instead, we focused on the dynamic power consumption of the TSV-based I/O channel. To estimate the dynamic power consumption of the TSV-based I/O channel, analytic models were proposed for calculating loading capacitances.
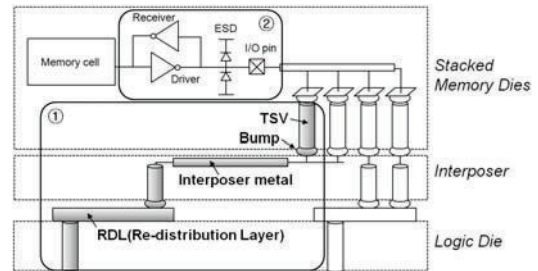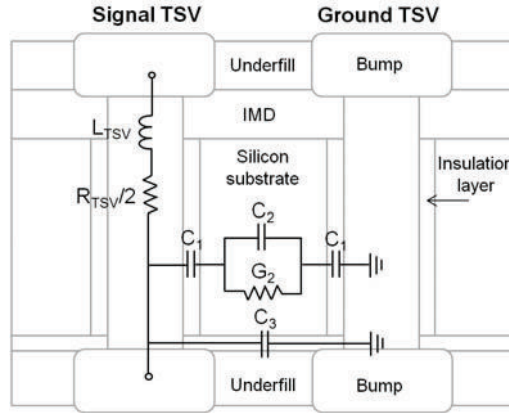

Fig. 1. Power consumption in a 3D IC; ① dynamic power consumption of TSV-based interconnect, ② dynamic/static power consumption of I/O circuitry.

Based on the proposed capacitance models, we estimated the dynamic power consumption of the TSV-based I/O channel and compared it for various 3D IC designs such as TSV arrays with different ground TSV counts, TSV and RDL/interposer metal dimension and various 3D architectures.

2. Proposed Model for Power Estimation of the TSV-based I/O Channel

As shown in Figure 2, the equivalent capacitance of a TSV, C_{TSV}, is proposed based on the equivalent-circuit model of TSV [1]. In this equivalent-circuit model, the bump effect is included as it is a necessary component for TSV connection between stacked dies. Due to the conductance of the silicon substrate between signal and ground TSVs, G_2, the equivalent capacitance of the TSV changes depending on frequency, which results in a slow-mode effect. In addition, G_2 can be expressed with C_2 and material properties such as an electrical permittivity of the silicon substrate, ϵ, and a conductivity of the silicon substrate, σ. Thus, the equivalent capacitance of the TSV, $C_{TSV(1S1G)}$, can be derived as a function of C_1, C_2, C_3 and material properties of the silicon substrate, which has a one-signal and one-ground TSV configuration (1S1G).

$$C_{TSV(1sng)}(\omega) = \frac{\alpha_n \cdot C_1 C_2 \left(\beta_n + \dfrac{\sigma}{\beta_n \cdot \varepsilon \omega} \right)}{\alpha_n \cdot C_1 + (\alpha_n + 1) \cdot C_2 \left(\beta_n + \dfrac{\sigma}{\beta_n \cdot \varepsilon \omega} \right)} + \alpha_n \cdot C_3$$

Fig. 2   A cross-sectional structure with the simplified equivalent-circuit model of a TSV, including a signal TSV, a ground TSV and bumps and the equivalent capacitance equation of a TSV.
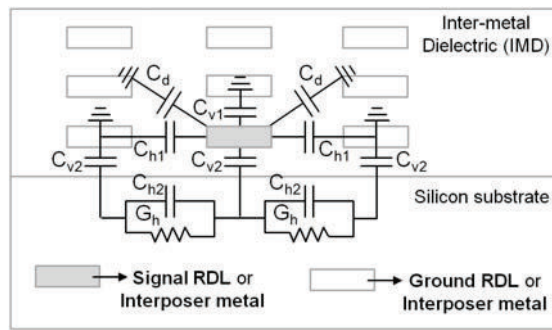
$$C_{RDL,bottom}(\omega) = \frac{2C_{v2}C_{h2}\left(2 + \dfrac{\sigma}{2 \cdot \varepsilon \omega} \right)}{2C_{v2} + 3C_{h2}\left(2 + \dfrac{\sigma}{2 \cdot \varepsilon \omega} \right)} + C_{v1} + 2(C_d + C_{h1})$$

Fig. 3 A cross-sectional structure of the RDL or interposer metal and its parasitic capacitances when signal propagates through the bottom metal layer, which is the closest layer to the silicon substrate, and the equivalent capacitance of a RDL.

3. Results and Discussion

With the 1s8g configuration, the changes in dynamic power consumptions with TSV dimension variation were calculated; here, TSV diameter (d_{TSV}), TSV pitch (p_{TSV}) and insulation layer thickness (t_{ox}) were the main design parameters for dimension variation of the TSV. As shown in Figure 4 $P_{d,TSV}$ increased as d_{TSV} was increased and as p_{TSV} and t_{ox} was decreased. Because C_1 and C_2 in Figure 2 both increased as d_{TSV} was increased. In addition, C_2 and C_3 increased as p_{TSV} was decreased and C_1 increased as t_{ox} was decreased, causing $P_{d,TSV}$ to increase.

Thus, to decrease d_{TSV} and to increase p_{TSV} and t_{ox} are the ways to reduce the dynamic power dissipation from the TSV, since they can reduce the equivalent
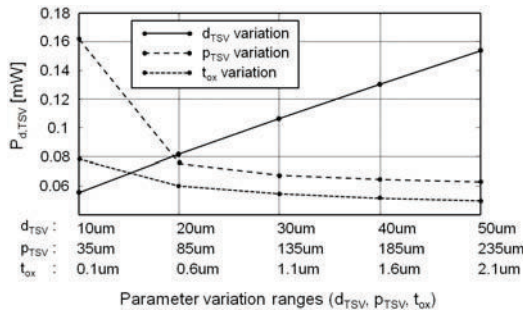
Fig. 4 Dynamic power consumption of TSV with d_{TSV} variation (p_{TSV}=135 μm, t_{ox}=0.5 μm), p_{TSV} variation(d_{TSV}=10 μm, t_{ox}=0.5 μm), t_{ox} variation (d_{TSV}=10 μm, p_{TSV}=35 μm) with the activity factor, supply voltage and operating frequency assumed to be 0.15, 1.2 V and 800 MHz, respectively.
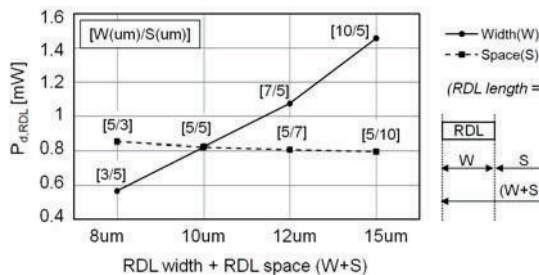

Fig. 5 Comparison of the dynamic power consumption of RDL, $P_{d,RDL}$, depending on width(W) and space(S) variation with the activity factor, supply voltage and operating frequency assumed to be 0.15, 1.2 V and 800 MHz.

capacitance of TSV, C_{TSV}.

To redistribute the I/O signals horizontally, RDL and interposer metal routing must be done within design parameters such as metal width (W), space (S), thickness (T), inter-layer dielectric (ILD) height (H), and length (L). Here, we estimated and compared the dynamic power consumption with variations in these parameters. As shown in Figure 5 the dynamic power consumption was more significantly influenced by width variation rather than space variation between RDLs. This is because the parasitic capacitance of an RDL is dominantly formed by the vertically confronting faces between RDLs or between the RDL and the silicon substrate. In the case of the interposer metal, power consumption was also more strongly affected by width than by space in the same manner as in the RDL case. This conclusion is only valid when the aspect ratio (W/T) is larger than 1. If not, S becomes more dominant in the dynamic power consumption rather than W. Thus, to decrease W and to increase S are the ways to reduce the dynamic power consumption from the RDL/interposer metal.

4. Conclusion

In this work, we proposed a capacitance model for a TSV-based I/O channel including TSVs, bumps, the RDL and interposer metal to estimate dynamic power consumption of a TSV-based I/O channel in a 3D IC. With the proposed model, we estimated and compared dynamic power consumption depending on TSV / RDL / interposer metal dimensional variations. Among the TSV-based I/O channel components, the dynamic power consumption was dominated by the RDL, and design guides of each component to save power were proposed.

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Vertical Noise Coupling on Wideband Low Noise Amplifier from On-chip Switching-Mode DC-DC Converter in 3D-IC

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Abstract— **3D-IC mixed-signal systems introduce vertical noise coupling which is a new noise coupling path by near-field coupling between logic ICs and RF/analog ICs. To guarantee the performance of the system, we should be aware of the amount of the vertical noise coupling during the system design stage. This paper reports the frequency-domain and time-domain measurement results of the vertical noise coupling on wideband low noise amplifier (LNA) from 200MHz on-chip switching-mode DC-DC converter in 3D-IC configuration. In the measurements from test vehicles with variations in stacking position and stack-up of the silicon substrate of the LNA, the vertically coupled noise is serious enough to obstruct the RF receiver operation; up to 80mV$_{pp}$ and 500mV$_{pp}$ of noise are vertically coupled across each inductor and at signal output of the LNA, respectively. The vertical noise coupling measurement results of this paper awake the seriousness of the vertical noise coupling issue in 3D-IC mixed-signal systems and can be a reference for the estimation of amount of vertical noise coupling in 3D-IC mixed-signal system design.**

Keywords-component; Vertical noise coupling; 3D-IC; On-chip switching DC-DC converter; Low noise amplifier (LNA)

I. INTRODUCTION

3D-IC is a new promising technology for designing a mixed-signal system. 2D System-on-Chip (SoC) integration of mixed-signal signal system has been using deep-submicron CMOS technologies due to its large scale integration and low cost. However, the deeply scaled CMOS technologies have many limitations for designing RF/analog circuits such as leakage, low gain and more process variations due to reduced supply voltage [1]. The 3D-IC technology resolves the problems by enabling technology mix same as System-in-Package (SiP) technology. We can use proper technologies for each of digital and RF/analog circuits. In the same time 3D-IC technology provides much smaller form factors than using SiP technology in the mixed-signal system design. These are great advantages in an optimization of the performance, size and cost of the mixed-signal system. However, in 3D-IC mixed-signal system, a new unanticipated noise coupling path by near field coupling between logic ICs and RF/analog ICs is introduced. Previous researches [2,3] report that serious noise can vertically couple between stacked-chips by near-field coupling

as shown in Fig. 1. The noise coupling can be more severe in 3D-IC than 2D SoC since several hundreds of μm distance between digital and sensitive RF/analog circuits in 2D SoC, Fig. 1 (a), is reduced to only a few tens of μm, Fig. 1 (b), between stacked digital and sensitive RF/analog chips.
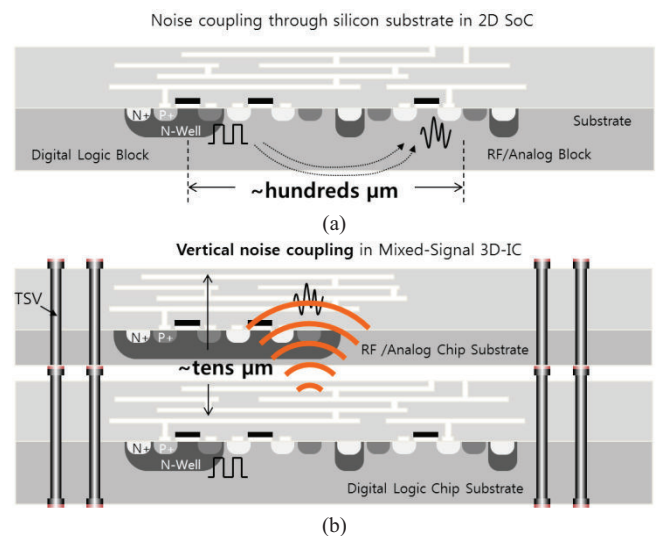

Figure 1. (a) Substrate noise coupling in mixed-signal system in 2D SOC (b) Vertical noise coupling between stacked digital and sensitive RF/analog chips of mixed-signal system in 3D-IC by near-field coupling

In this paper, the frequency domain and time-domain measurement result of the vertical noise coupling on wideband low noise amplifier (LNA) from 200MHz on-chip switching-mode DC-DC converter in 3D-IC configuration are reported. Chapter II describes various test vehicle designs for the measurement; variations in stacking position of top-chip in 3D-IC configuration and stack-up of the silicon substrate of the LNA. Chapter III presents, first, measured vertical transfer impedances between the noise source in the on-chip DC-DC converter and inductors of the LNA up to 10GHz at those test vehicles using on-chip probes. Then, measured vertically coupled noises across the inductors of the LNA and at the LNA output are presented. The measurement results of this paper reveal the seriousness of the vertical noise coupling issue in

3D-IC mixed-signal systems and can be a reference for the estimation of amount of vertical noise coupling in 3D-IC mixed-signal system design.

II. TEST VEHICLE DESIGN

A. 200MHz On-chip DC-DC Converter Design

Fig. 2 depicts the schematic and chip-photo of the power stage of 200MHz on-chip DC-DC converter. It is a synchronous buck switching DC-DC converter. Table I summarizes the measured performance of the DC-DC converter. Including 37nH on-chip spiral inductor and 2.5nF on-chip filter capacitor, all components of the power stage are integrated in the chip.
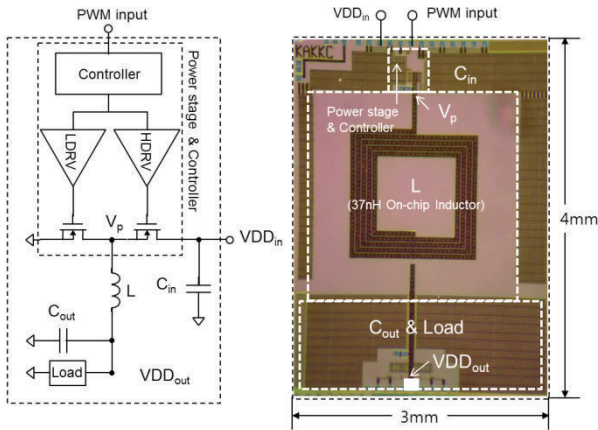
Figure 2. Schematic and chip-photo of 200MHz on-chip DC-DC converter

TABLE I. MEASURED PERFORMANCE OF ON-CHIP DC-DC CONVERTER

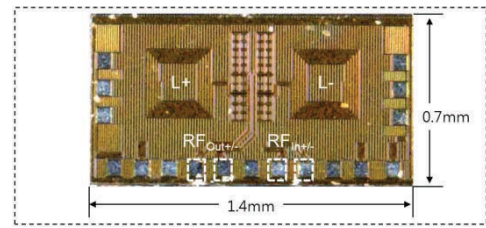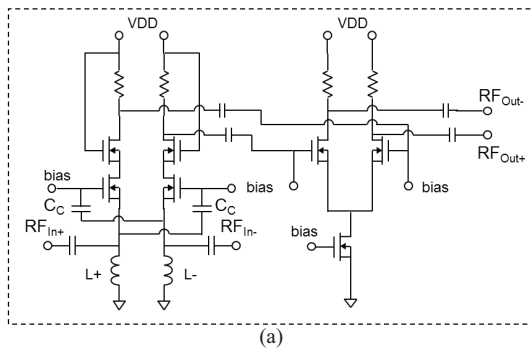| Technology	CMOS 6M1P 0.18μm
Switching Frequency	200MHz
VDD_{in}/VDD_{out}	3.3V / 0.6~2.5V
Max. I_{out} / Min. I_{out}	200mA / 60mA
Max. V_{ripple}	<70mVpp
Max. Power Conversion Efficiency	~63%

B. Wideband LNA Design

(a)
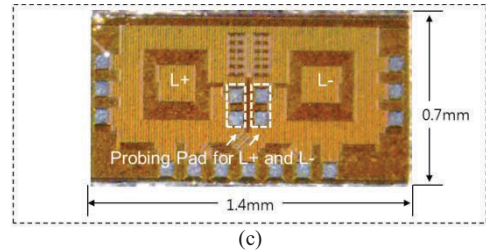
Figure 3. (a) Schematic and (b) chip-photo of wideband LNA (c) chip-photo of inductors of wideband LNA for vertical noise coupling measurement

TABLE II. MEASURED PERFORMANCE OF WIDEBAND LNA

Technology	CMOS 6M1P 0.18μm
Operation Frequency Band	600M~3GHz
In/Output Matching	<-10dB
Noise Figure	~2.7dB
Gain	10~14dB
IP3 (input)	5.1dBm
P1dB	-5.02dBm

The schematic and chip-photo of wideband LNA are shown in Fig. 3 (a) and (b). The LNA is cross-coupled differential common-gate LNA [4]. It is applicable for 900MHz, 2.4GHz ISM band applications. Table II summarizes the measured performance of the wideband LNA. In the LNA chip shown in Fig. 3 (c), inductors of wideband LNA, L+ and L- in Fig. 3 (a), are disconnected from the actives and have probing pads for vertical noise coupling measurement on-chip.

C. Final Test Vehicle

The final test vehicle is PCB mounted 2-chip stacked 3D-IC as shown in Fig. 4 (a) and (b). The LNA chip is stacked on the on-chip DC-DC converter with 20μm epoxy adhesive. There are 3 types of variations in the final test vehicles. First, it is in the type of LNA chips. $TV_{coupling}$ set in Fig. 4 (a) uses the chip in Fig. 3 (c), which only contains inductors for LNA, as the top-chip. TV_{LNAout} set in Fig. 4 (b) uses the chip in Fig. 3 (b), which contains full LNA circuit. $TV_{coupling}$ set is for a direct measurement of the vertical noise coupling from V_p of the on-chip DC-DC converter to L+,L- of the LNA using on-chip probing. In TV_{LNAout} set, we measure vertically coupled noise at off-chip LNA output from the on-chip DC-DC converter switching in time-domain. Second, the variation is in the thickness of silicon substrate of the LNA. The silicon substrate of the LNA is thinned to be 50μm in TV_{50u} and 100μm in TV_{100u} as shown in Fig. 4(b). This variation is to measure the

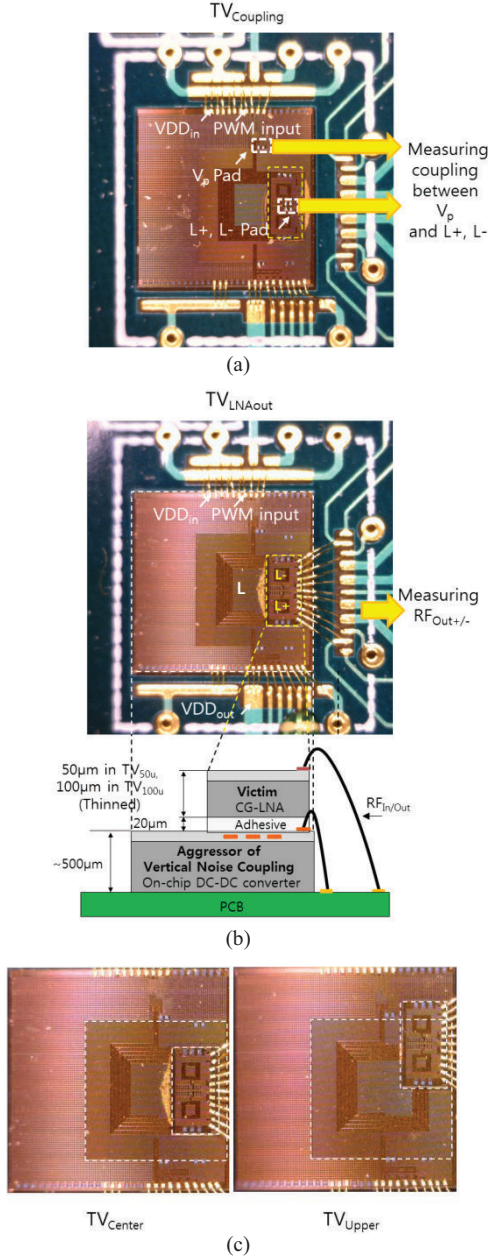impact of silicon substrate thickness of victim chip on the amount of vertical noise coupling.

(a)

(b)

(c)

Figure 4. Chip-photo and cross-section of final test vehicles: 2-chip stacked 3D-IC (a) $TV_{coupling}$: Test vehicle for vertical noise coupling measurement from V_p to L+/L- (b) TV_{LNAout} : Test vehicle for measurement of vertically coupled noise at LNA output ($RF_{Out+/-}$) (c) TV_{Center}, TV_{Upper} : Test vehicles with variation in the position of the top chip (LNA)

TABLE III.   FINAL TEST VEHICLE SETS

Description of test vehicle set	Notation of test vehicle set
Variation in LNA chip	$TV_{Coupling/LNAout}$
Variation in silicon substrate thickness of the LNA chip	$TV_{50u/100u}$
Variation in stacking position of the LNA chip	$TV_{Center/Upper}$
Example of the name of final test vehicle	$TV_{Coupling/50u/Center}$

For the last, the variation is in the stacking position of the top chip (LNA) as shown in Fig. 4 (c). The description of the final test vehicles and their names are summarized in Table III. All the input/output signal of the LNA and the DC-DC converter is wire-bonded out to the off-chip PCB. The PCB is a simple pair of power/ground plane. There is no electrical connection through the adhesive between the on-chip DC-DC converter and the LNA.

III.   MEASUREMENT OF VERTICAL NOISE COUPLING

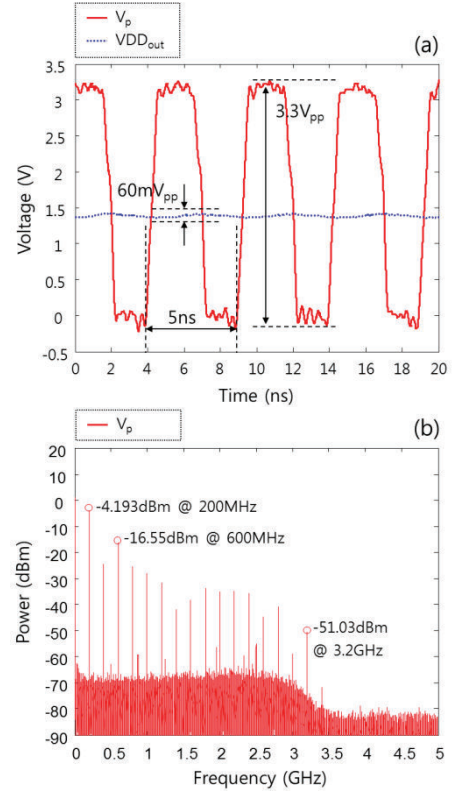A. Source of Vertical Noise Coupling

Figure 5. (a) Measured switching voltage at V_p and DC output at VDD_{out} of the on-chip DC-DC converter with high-Z on-chip probe (b) Existence of high frequency component up to 3.2GHz in the power spectrum of the switching voltage at V_p

It is well known that the switching of the on-chip switching DC-DC converter is the #1 source of EMI [2]. Accordingly, the source of vertical noise coupling in the 200MHz on-chip DC-DC converter is switching at V_p. Fig. 5 (a) shows the measured voltage of switching at V_p and DC output voltage at VDD_{out} with high-Z on-chip probe. At V_p, there is 3.3V 200MHz switching with duty of PWM input of the on-chip DC-DC converter. In the measurement setup, the PWM input has half duty and the load at the output is 18ohm. Accordingly, the DC output voltage at VDD_{out} becomes ~1.5V with 60mV$_{pp}$ voltage ripple. Due to parasitic series inductance of input decoupling capacitors and on-chip interconnections to off-chip VDD_{in}, some ringing are found in the switching waveform of V_p. Noticeable frequency spectrum components exist up to 3.2GHz as shown in Fig. 5 (b).

B. Direct Measurement of Vertical Noise Coupling from V_p of the On-chip DC-DC Converter to Inductors of LNA

1) In Frequency Domain: The switching at V_p is vertically coupled mainly to the inductors, L+ and L-, of the LNA [2]. It is an inductive coupling since a capacitive coupling is negligibly small due to the grounded substrate of the LNA [3]. The inductive coupling from V_p to bond-wires of LNA is also ignored since it is negligibly small due to following reasons; 1) they are vertically farther away than the L+ and L- from the V_p and L 2) the direction of bond-wires is perpendicular to the direction of inductor current at the right side of L.The vertical noise coupling from V_p, noise source, of the on-chip DC-DC converter to L+ and L- , noise victims, in the $TV_{Coupling}$ set are measured in terms of transfer impedance from 1MHz to 10GHz using 2-port Vector Network Analyzer and 50 Ω on-chip probes. Fig. 6 plots the transfer impedance from V_p to L+,L- in $TV_{Coupling/50u/Center}$. We choose transfer impedance instead of s-parameter to evaluate the amount of veritcal coupling since s-parameter assumes 50 Ω termination at every ports, which is not a realistic situation in an on-chip circuit. The transfer impedance measurement cannot be done under time-variant condition such as switching events at the on-chip DC-DC converter. In that reason, we measure the transfer impedance at 2 equivalent switching conditions of on-chip DC-DC converter: HDRV on, LDRV off and HDRV off, LDRV on. HDRV on, LDRV off condition is when the switching at V_p goes to 3.3V from 0V. The high-side driver, HDRV in Fugire 2, turns on and the low-side driver, LDRV, turns off in that case. In the same manner, HDRV off, LDRV on equals to the falling of the switching at V_p.
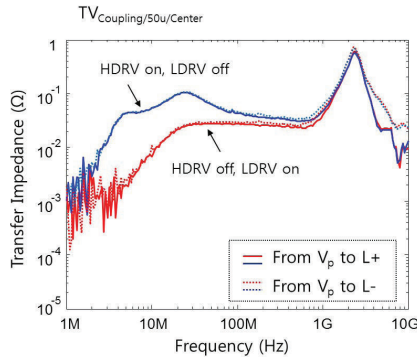
Figure 6.   Measured vertical transfer impedance from V_p to L+/- in $TV_{Coupling/50u/Center}$ from 2-port VNA measurement

In Fig. 6, we found that the HDRV on, LDRV off condition shows larger and inductive transfer impedance than HDRV off, LDRV on conditon in the 200MHz to 1GHz frequency band. From the result, we can expect that there will be more vertical noise coupling at the rising of the 200MHz switching, up to 5th harmonics of the fundamental switching frequency component of the on-chip DC-DC converter. The peak around 2GHz is from the resonance due to inductance of L+/L- and capacitance reference to the silicon substrate. The transfer impedance from V_p to L+, solid lines, and from V_p to L-, dashed lines, do not different in the magnitude since the

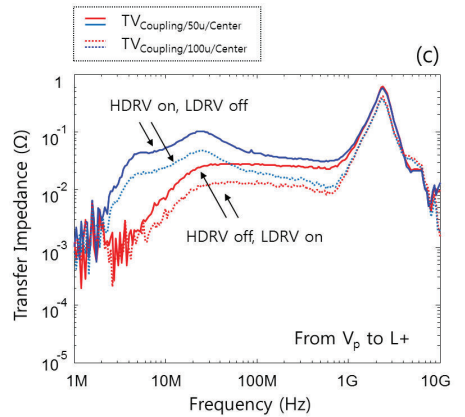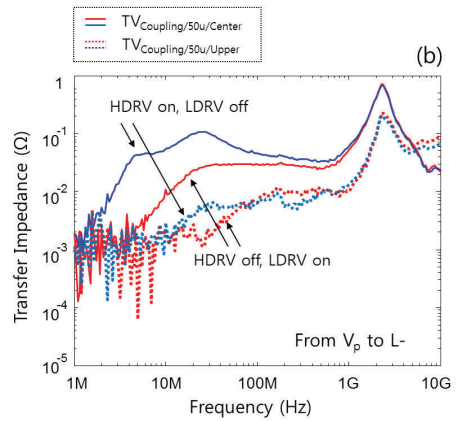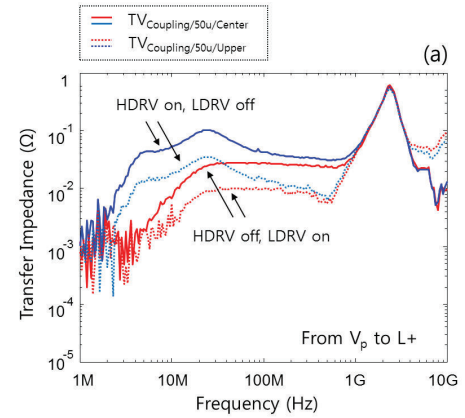L+ and L- are symmetrically located to the center of the inductor, L, of the on-chip DC-DC converter.

In Fig. 7 (a) and (b), we change the stacking position of the top chip, LNA. $TV_{Coupling/50u/Center}$ shows larger transfer impedance in 200MHz to 1GHz frequency band than $TV_{Coupling/50u/Upper}$ in both cases: from V_p to L+ and from V_p to L-. The difference between 2 TVs are greater in case of from V_p to L-. This is natural since L+ and L- are moved away from the center of the L in $TV_{Coupling/50u/Upper}$ and L- is the one which is moved farther away as depicted in Fig. 4 (c). The mutual inductances extracted from the measurements are 1.1nH from V_p to L+ and from V_p to L- of $TV_{Coupling/50u/Center}$. It is 0.35nH/0.08nH from V_p to L+ and from V_p to L- of $TV_{Coupling/50u/Upper}$, respectively.

In Fig. 7 (c) and (d), $TV_{Coupling/100u/Center}$ shows less inductive transfer impedance in 200MHz to 1GHz frequency band than $TV_{Coupling/50u/Upper}$ in both cases: from V_p to L+ and from V_p to L-. 50μm thicker silicon substrate of $TV_{Coupling/100u/Center}$ secures more distance from V_p to L+/L-. The mutual inductances extracted from the measurements are 0.5nH from V_p to L+ and from V_p to L- of $TV_{Coupling/100u/Center}$. However, the transfer impedance over 1GHz frequency has relatively less changes than that of 200MHz to 1GHz frequency band. The transfer impedance over 1GHz frequency is capacitive rather than inductive. The capacitive coupling is less sensitive to the changes in thickness of silicon substrate of the LNA due to bulk conductivity of the silicon substrate [5].

2) In Time Domain: Fig. 8 (a), (b) and (c) plot measured vertically coupled noise across inductors of the LNA, L+/-, from the on-chip DC-DC converter switching in $TV_{Coupling/50u/Center}$, $TV_{Coupling/50u/Upper}$ and $TV_{Coupling/100u/Center}$, respectively. In $TV_{Coupling/50u/Center}$, the vertically coupled noise across L+ and L- are having almost same amplitude, about 80mV_{pp}, but out-of-phased. This is because L+ and L- are mirror symmetric to the center of the inductor, L, of the on-chip DC-DC converter. The polartiy of mutual inductance to L+ and L- are opposite. The polarity is also opssite in $TV_{Coupling/100u/Center}$ in Fig. 8 (c). Only the amplitude of the vertically coupled noise across inductors has been reduced to 36/31.5mV_{pp} for L+ and L-, respectively. This change is easily understandable from the direct measurement of vertical noise coupling in Fig. 7 (c),(d). In case of $TV_{Coupling/50u/Upper}$ in Fig. 8 (b), the vertically coupled noise across L+ and L- are in-phased. This is because the L+ and L- are having same polartiy of mutual inductance to the inductor L since both of them are placed at the outter side of the inductor L of the on-chip DC-DC converter. It shows that there can be some optimal placement of inductors to make the vertically coupled noise across the inductors a common-mode. Since the LNA is fully balanced, the common-mode vertically coupled noise will be canceled out at the differential LNA output. This is one of the soulution to minimize the impact of vertical noise coupling on the LNA.
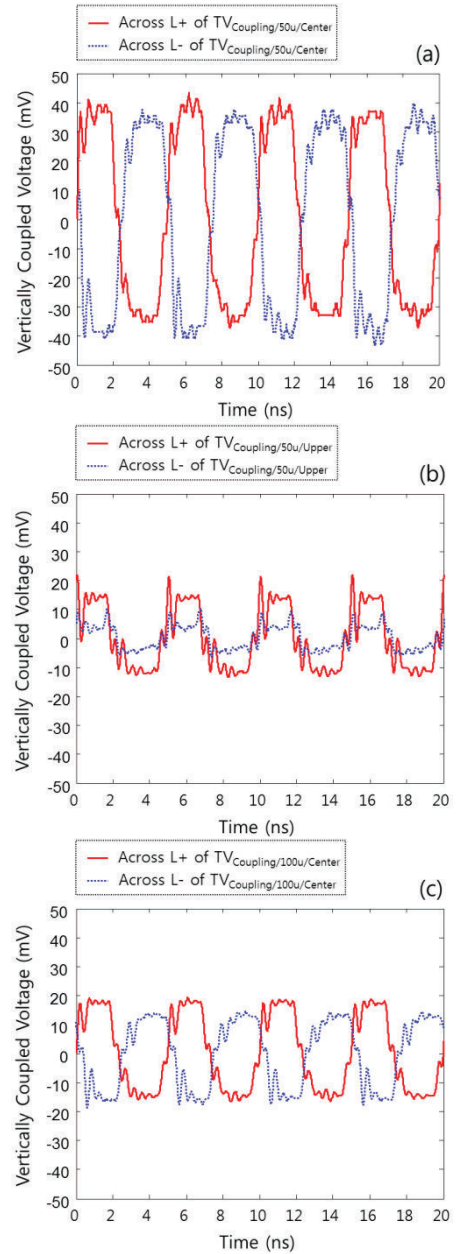

Figure 8. Measured vertically coupled noise across L+/- from the on-chip DC-DC converter switching in (a) $TV_{Coupling/50u/Center}$ (b) $TV_{Coupling/50u/Upper}$ (c) $TV_{Coupling/100u/Center}$

C. Vertical Noise Coupling at LNA Output ($RF_{Out+/-}$)

Fig. 9 plots measured vertically coupled noise at LNA output, $RF_{Out+/-}$, from the on-chip DC-DC converter switching in $TV_{Coupling/50u/Center}$, $TV_{Coupling/50u/Upper}$ and $TV_{Coupling/100u/Center}$. LNA inputs are all 50Ω terminated without RF signal input to measure a pure vertically coupled noise at the LNA output. Due to the cross-coupled capacitor, C_C in Fig. 3 (a), the vertically coupled noise at RF_{out+} and RF_{out-} are out-of-phased and have balanced amplitude even in $TV_{Coupling/50u/Upper}$, which shows in-phased and imbalanced vertically coupled noise across L+ and L-. The vertically coupled noise at LNA output is ranged from 100mV_{pp} to 500mV_{pp}. This amount is much larger than the vertically coupled noise across L+ and L- in Fig.

8. That is because LNA circuit amplifies the vertically coupled noise across L+ and L-. Table IV summarizes the measured peak to peak vertically coupled noise.
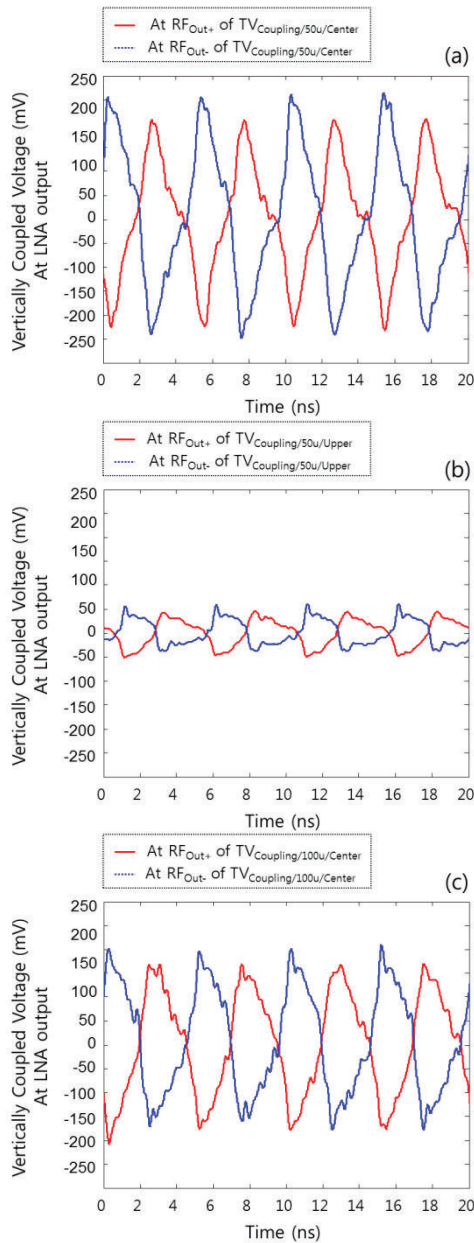

Figure 9.   Measured vertically coupled noise at LNA output (RF$_{Out+/-}$) from the on-chip DC-DC converter switching in (a) TV$_{Coupling/50u/Center}$ (b) TV$_{Coupling/50u/Upper}$ (c) TV$_{Coupling/100u/Center}$

TABLE IV.   SUMMARY OF THE MEASURED PEAK-TO-PEAK VERTICALLY COUPLED NOISE AT WIDEBAND LNA FROM ON-CHIP DC-DC CONVERTER

	Across inductor sof LNA(mV$_{pp}$)		At LNA output (mV$_{pp}$)	
	L+	L-	RF$_{Out+}$	RF$_{Out-}$
TV$_{Coupling/50u/Center}$	80.5	78.5	449.9	506.89
TV$_{Coupling/50u/Upper}$	35	16.5	97.6	100.6
TV$_{Coupling/100u/Center}$	36	31.6	365.83	390.8

IV.   CONCLUSION

In this paper, the frequency domain and time-domain measurement results of the vertical noise coupling on wideband LNA from 200MHz on-chip switching-mode DC-DC converter in 3D-IC configuration are reported. The test vehicles have variations in stacking position and stack-up of the silicon substrate of the LNA. The frequency domain measurement results tell that the vertical noise coupling is inductive dominant below 1GHz. From 3.3V 200MHz switching of the on-chip DC-DC converter, measured vertically coupled noise is up to 80mV$_{pp}$ and 500mV$_{pp}$ across each inductor and at LNA output, respectively. Considering a typical RF signal of several tens of mV$_{pp}$ in LNA output stage, it is clear that the vertical noise coupling can cause serious problem in the RF receiver operation. The vertical noise coupling measurement results of this paper awake the seriousness of the vertical noise coupling issue in 3D-IC mixed-signal systems and can be a reference for the estimation of amount of vertical noise coupling in 3D-IC mixed-signal system design.

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