Synthesis and Characteristics of Au/Ga_2O_3 Core-shell and Peapod Nanostructures

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Abstract

Core-shell nanowires have attracted much attention for their interesting electrical properties. With Ga metal source, Au/Ga_2O_3 nanowires were synthesized on silica substrate via the vapor-liquid-vapor (VLS) growth mechanism in the chemical vapor deposition (CVD) system. According to the results examined by HRTEM and FESEM, the as-grown Ga_2O_3 nanowires are single crystal with Au at the center. And through the current-voltage measurement , we find out the resistive switching characteristic of the core-shell Au/Ga_2O_3 nanowires. Furthermore, by thermal annealing, the core-shell Au/Ga_2O_3 nanowires were successfully transformed into gold-peapodded Ga_2O_3 nanostructures. In addition, the size, shape, and interspacing between the particles can be manipulated by varying the annealing time. These results may apply on the diverse applications in optoelectronics and biosensor devices with 1D nanostructures.

1. Introduction

Nanoscale materials and devices have attracted much attention for their interesting and special properties to the potential applications in various fields (1-2). Among these nanostructures, 1-D nanomaterials have shown many promising potential applications such as functional unit in fabricating nanoscale electronics, optoelectronic, electrochemical and electromechanical devices (3-6). Nowadays, the growth mechanisms for synthesizing one-dimensional nanostructures have been published a lot , including vapor-liquid-vapor (VLS), vapor-solid (VS), solution-liquid-solid (SLS), oxide-assisted (OA) growth mechanisms and so on (7-9).

In this study, core-shell Au/Ga_2O_3 nanowires were synthesized and their electrical properties were investigated. Due to its unique transparent property, core-shell Au/Ga_2O_3 nanowire is one of the most interesting materials.

To well control the dimension of the nanowires, VLS growth mechanism in the CVD system was applied to fabricate the nanowires (10-11). Through the mechanism, metal was employed as the catalyst, forming an active liquid alloy droplet in the vapor phase ambiance with reactants. As the droplet becomes supersaturated, nucleation and crystal growth occurs until the reactant is exhausted.

Subsequently the core-shell nanowires were annealed to form peapod structures by the mechanism of Rayleigh instability. The driving force of Rayleigh instability is to decrease the surface area and the total surface energy.

2. Experimental Section

Au/Ga_2O_3 nanowires were synthesized on silica substrate with Ga slugs as material sources via physical evaporation methods. Then the silica substrates were respectively placed in a horizontal quartz tube furnace. The three zone reaction temperature was set at 800°C under 0.01Torr with controlled reaction time, then cool to room temperature. After the core-shell nanowires were synthesized, the field emission scanning electron microscope and the field emission transmission electron microscope were used respectively to analyze the morphology of nanowires, the crystal structures and chemical compositions of nanowires.

Final we use the optical microscope with manipulator and a series of standard electron beam lithography (EBL) techniques to fabricate the nanodevice. Then the Keithley 4200, which was equipped with optical microscope, was applied to analyze the current-voltage (I-V) measurement.

On the other hand, for in situ TEM

observation of the peapod structure, Jeol 2000V UHV-TEM was used in this study. The samples were heated in a double tilt heating holder inserted into the electron beam path of the TEM and the real time behavior was recorded by video.

3. Results and Discussion

In order to get high density of the Au/Ga_2O_3 core-shell nanowires, we have tried various duration time and cooling time, while all the reaction temperature and pressure was kept at 800° C and $1x10^{-2}$ torr separately. After various trials, we finally can control the length and the diameter of the Au/Ga_2O_3 core-shell nanowires by using different size Au catalyst and time conditions. The surface morphology of the Au/Ga_2O_3 core-shell nanowires are as shown in Figure 1. It shows that the FESEM image of high density Au/Ga_2O_3 nanowires with very uniform diameter fabricated by 150nm Au catalyst.

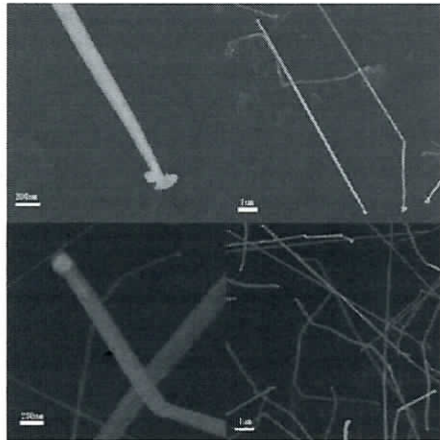

Figure 1. FESEM images of the Au/Ga_2O_3 nanowires synthesized by 150nm Au nanoparticles.

A low-magnification FETEM image of a single Au/Ga_2O_3 nanowire is as showed in Figure 2 (a). It can strongly prove that the Au/Ga_2O_3 core-shell nanowires were fabricated through Au catalysts and the diameters were relative to the Au nanoparticles size. Figure 2(b) illustrates the high resolution FETEM image of the Au/Ga_2O_3 nanowire. It indicated that the zone axis of Au/Ga_2O_3 nanowire was in [152] direction. And Figure 2(c) is the corresponding diffraction pattern (DP); Figure 2(d) shows the STEM image with composition profile, we can clearly see that the Au is at the center with the Ga_2O_3 shell.

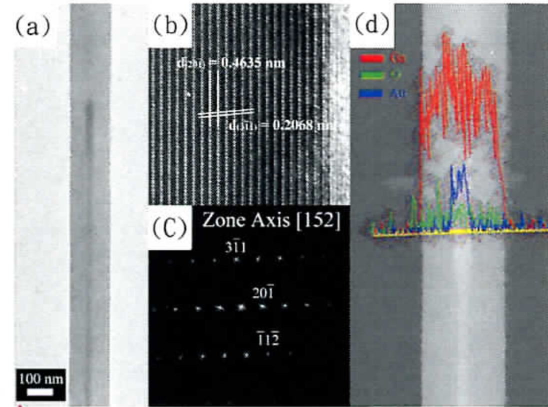

Figure 2. (a) Low-magnification TEM image (b) High resolution TEM image. It shows the spacing of (201) plane was 0.4635 nm and the spacing of (311) plane was 0.2068 nm, respectively. (c) Shows the corresponding diffraction pattern (DP). (d) composition profile identification by linescan of EDX

The Au/Ga_2O_3 core-shell nanowire exhibits the resistive switching characteristics as shown in Figure 3. The set switching (HRS→LRS) and the reset switching (LRS→HRS) could be identified as bipolar switching mode. Moreover, the operating resistive switching current can be at micro amp, thus it has the potential to be applied on resistive random access memory (RRAM).

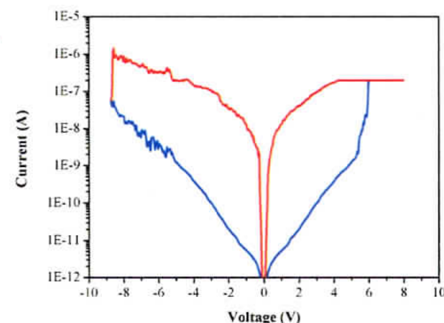

Figure 3. The resistive characteristic of the core-shell Au/Ga_2O_3 nanowires.

Furthermore, the nanowires were found to be transformed into peapod structures by anneal process. To study the structural changes as a function of temperature, the nanowires were annealed isothermally at 600 and 850 ° C for 30 min, as shown in Figure 4. After annealing at 850° C for 30 min, the nanowire was fragmented into nanoparticle chains along the whole length of itself.

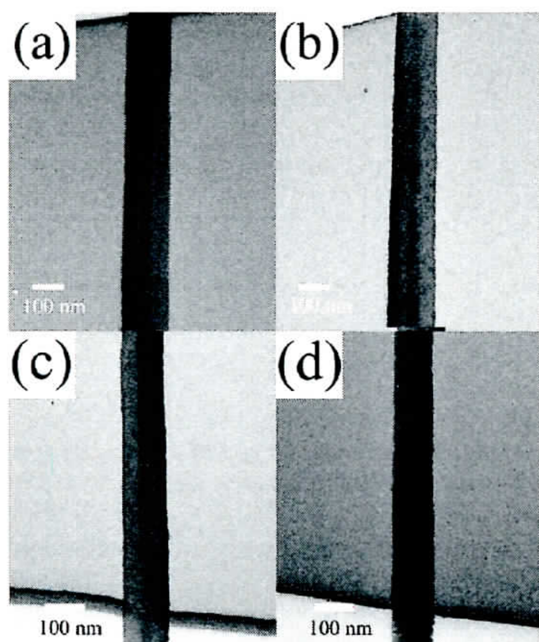

Figure 4.
(a)(b)SEM images of core-shell nanowires before and after annealing at 600 ° C. (c)(d)SEM images of core-shell nanowires before and after annealing at 800° C

4. Conclusion

In summary, core-shell nanowires have attracted much attention for their interesting electrical properties. According to the results examined by HRTEM and FESEM, the as-grown Ga_2O_3 nanowires are single crystal with Au at the center. The growth of Au/Ga_2O_3 core-shell nanowires obeys the VLS mechanism owing to the gold nanoparticles at the tip region of nanowires. Through the current-voltage measurement, we indeed find out the resistive switching characteristic of the core-shell Au/Ga_2O_3 nanowires, thus it has the potential to be applied on resistive random access memory.

And through anneal process the core-shell nanowires were changed to form peapod structures by the mechanism of Rayleigh instability. The driving force of Rayleigh instability is to decrease the surface area and the total surface energy.

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Direct Observation of Nanofilaments in BMO Resistive Switching Memory

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Abstract

Resistance random access memory devices based on metal oxides could be a potential candidate for next-generation non-volatile memory (NVM). Although the resistive switching behaviors have been widely studied in previous reports, the real switching mechanism is still unknown. There are still several types of filament formation mechanisms being proposed but are only characterized indirectly. In this study, a new type of nanofilament, which is proven to be pure metals (Mn and Bi) characterized using high-resolution transmission electron microscopy (HRTEM) in Pt/BMO/Pt devices which examined the electrical properties exhibit stable and reproducible bipolar resistive switching behavior with great endurance and retention properties. In addition, the formation of nanofilament is probably due to an electrical-driving reductive mechanism during the set processes. The high-density metallic nanofilaments indicate that the BMO thin film could reduce the cell size which can be successfully demonstrated by cross-bar structure. The Pt/BMO/Pt device reveals high potential for high-density NVM applications.

1. Introduction

Resistance random access memory (RRAM) devices based on metal oxides could be a potential candidate for next-generation non-volatile memory (NVM). Although the resistive switching behavior has been widely studied in previous reports, and it is clear that the switching mechanism is due to the formation and rupture of conductive nanofilaments within the insulating layer, but the real formation mechanism is still unknown. There are several types of filament formation mechanisms being proposed, but mostly are characterized indirectly, and thus lack of precise information about the real formation of the filaments. On the other side, the conductive bridge[1,2] and phase change[3] systems have attracted considerable attention since they have been observed experimentally. Conductive bridge RAM is based on a solid-state electrolyte in which mobile metal ions create a conductive bridge between the two electrodes under the influence of an electric field. The mechanism of conducting bridge system has been reported by in situ observation of voltage-induced changes in the microstructure of a solid electrolyte memory such as the Pt-Ir/Cu-GeTe/Cu structure.[2] Phase change RAM employs the difference in resistivity between the different crystalline phases of a compound. The phase change phenomenon such as TiO_2 being transformed to Ti_4O_7 by the external field and thermal effects had also been directly observed by in-situ transmission electron microscopy in

Pt/TiO_2/Pt structure.[3] Therefore, this study inspect the real formation of a new type of nanofilament based on pure metals (Mn and Bi) and characterized by high-resolution transmission electron microscopy (HRTEM). Additionally, the resistive switching properties of Pt/BMO/Pt device are studied by electrical measurements. Stable and reproducible bipolar resistive switching characteristics are found with great endurance and retention properties. The formation of the nanofilament is probably due to an electrical-driving reductive mechanism during the set process. Finally, the direct observation of the nanofilament size about 10-20 nm indicates that the BMO thin film could be used for high density NVM applications.

2. Device Fabrication

BMO thin films of 70-nm thick were deposited on Pt/Ti/SiO2/Si substrates at 500°C by pulsed laser deposition. The crystal structure and microstructure were examined by x-ray diffraction (XRD) and high-resolution transmission electron microscopy (HRTEM), respectively. The current-voltage characteristics of the Pt/BMO/Pt device were also measured using a Keithley 4200 semiconductor parameter analyzer. All the measurements were performed at RT

3. Results and Discussion

The typical I-V characteristics of RRAM cell based on the Pt/BMO/Pt structure are shown in Fig. 1(a). The forming electric field of 0.257 MV/cm for Pt/BMO/Pt device was much lower than those reported in the literatures. Figure 1(b) shows the typical results of sweeping the current from 0 to 5 mA in the set process, while the sweeping voltage from 0 to -1 V in the reset process is maintained. Similar voltage switching conditions (V_{set} was about 1 V and V_{reset} was about -0.6 V) are exhibited in Fig. 1(a) and (b). Therefore, base on current sweeping results, there are clear advantages which are the spike phenomenon was avoided in the set process and the lower set and reset currents lead to lower power dissipation by performing current sweeping mode.

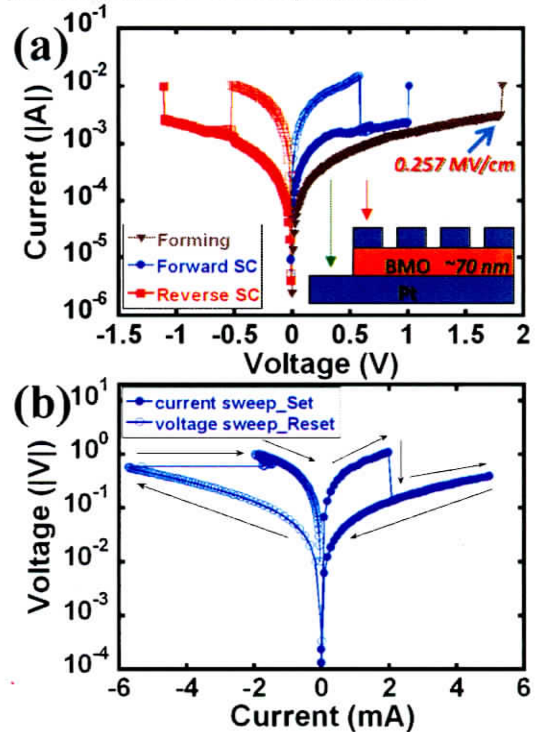

Fig. 1 (a) Typical I-V characteristics of the Pt/BMO/Pt device. The inset shows the structure of RRAM device which top electrode with a diameter about 200□ m. (b) I-V characteristics of resistive switching in current sweep process.

Figure 2(a) is a typical cross-sectional bright-field TEM image of the Pt/BMO/Pt device after the measurement, which is revealing the formation of several MNFs between the TE and BE after switching operation at RT, in addition, the intact nanofilaments connected TE and BE which were arrowed. Further analysis of the MNFs is characterized by the HRTEM image, illustrate the measured d-spacing of 0.315 nm corresponds to the Mn(022) planes in Fig. 2(b) and the other measured d-spacing of 0.373 nm corresponds to the Bi(011) planes in Fig. 2(c)

Finally, this study demonstrated the cross-bar structure device (2×2 μm^2) which is shown in the inset of Fig. 3 to prove the property of high MNFs density is beneficial for reducing the device size. The typical I-V characteristics of RRAM cell based on cross-bar structure were shown in Fig. 3, which illustrated the cross-bar structure device exhibited resistive switching behavior.

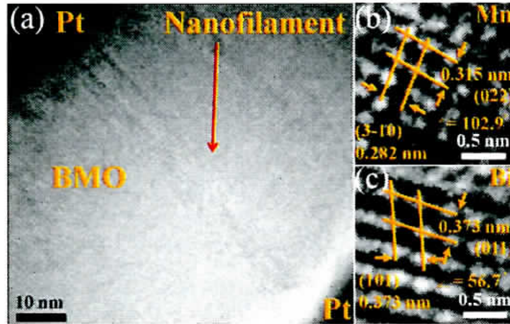

Fig. 2 (a) Cross-sectional TEM image of Pt/BMO/Pt device after forming process. (b) HRTEM images of the crystal Mn and (c) Bi in the nanofilament.

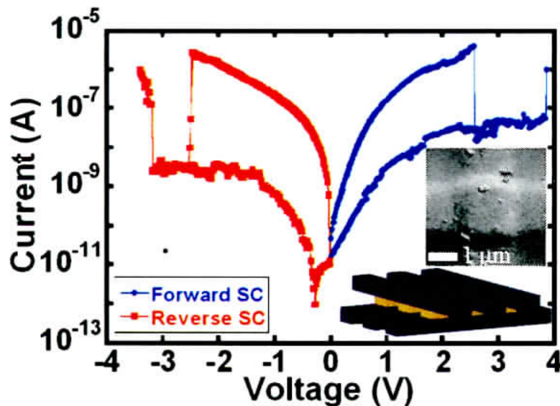

Fig. 3 Typical I-V characteristics of the Pt/BMO/Pt cross-bar structure. The inset shows the SEM image of single cell with an area about 2×2 μm^2

4. Conclusion

In conclusion, a preliminary investigation of BMO for nonvolatile memory applications has been performed for the first time. The Pt/BMO/Pt device showed low forming electric field, low power dissipation, in BOM. Although, the BOM with current and voltage sweeping mode in the set and reset process respectively was found to have lower power dissipation, than performing voltage sweeping in both reset and set modes. Based on the HRTEM analysis, the MNFs were formed by optimal deoxidization conditions in BMO thin film region. According to the property of high MNFs density, the device could reduce the cell size which can be successfully demonstrated by cross-bar structure. Therefore, the BMO layer exhibits the potential for ultrahigh storage density application. Further investigation should be conducted to understand the physics of set and reset transition processes, which is not clear yet. This paper brings up an exciting possibility of building next-generation memory devices by using BMO thin films.

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Bipolar Resistive Switching of Single Gold-in-Ga_2O_3 Nanowire

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Abstract

We have fabricated single nanowire chips on gold-in-Ga_2O_3 core -shell nanowires using the electron-beam lithography techniques and realized bipolar resistive switching characteristics having invariable set and reset voltages. We attribute the unique property of invariance to the built-in conduction path of gold core. This invariance allows us to fabricate many resistive switching cells with the same operating voltage by simple depositing repetitive metal electrodes along a single nanowire. Other characteristics of these core–shell resistive switching nanowires include comparable driving electric field with other thin film and nanowire devices and a remarkable on/off ratio more than 3 orders of magnitude at a low driving voltage of 2 V. A smaller but still impressive on/off ratio of 10 can be obtained at an even lower bias of 0.2 V. These characteristics of gold-in-Ga2O3 core–shell nanowires make fabrication of future high-density resistive memory devices possible.

1. Introduction

Resistive random access memory (RRAM) with a simple sandwich structure of metal/insulator/metal (MIM) is one of the emerging nonvolatile memory technologies which has great features such as faster writing speed, smaller device feature size, lower programming voltage and multistate memory[1,2] as compared to other counterparts. Resistive switching phenomena are found in perovskite oxides and binary transition metal oxides such as PCMO,[3] Cr-doped $SrZrO_3$,[4] NiO,[5] ZnO,[6] TiO_2,[7] and Nb_2O_5,[8] etc. Resistive switching characteristics can be classified into bipolar and unipolar switching types based on the set and reset processes controlled by the polarity or magnitude of the applying bias. Several mechanisms such as filamentary model,[9] charge-trap model,[10] and space-charge-limited current,[11] have been proposed to illustrate resistive switching characteristics but more in-depth investigations are still needed. Recently, riding with the revolution of nanotechnology and development of electron beam lithography, we have fabricated the electrical measurement chips on nanowires and assemble electronic or photonic devices beyond photolithographic limitation.[12,13] Making single-nanowire devices provides not only a controllable method to investigate the resistive switching mechanism at sublithographic scale but also a possible means to further increasing the density of memory cells.[14-16] For practical applications, reducing the operation current is important because higher current means higher power consumption and requires a larger chip size. The single-nanowire memory devices can reduce the operation current to nanoampere and lower the driving electric field to tens of kilovolts per centimeter.[17] Moreover, heterostructure nanowires have attracted considerable attention owing to their multifunctional characteristics and unique properties.[18-19] Gold-in-Ga_2O_3 core-shell and peapod nanowires can be synthesized in one-step process or two-step process with postannealing.[20,21] This unique nanowire, metal Au embedded in dielectric material Ga_2O_3, has special properties in photo response with specific wavelength.[22] In this study, we report for the first time a bipolar resistive switching behavior of a single gold-in-Ga_2O_3 core-shell nanowire. Conducting a thorough current-voltage analysis of the nanowire devices we have noticed a unique property that the set and reset voltages do not depend on the electrode distance. These results may be important to future nanodevices in resistive switching.

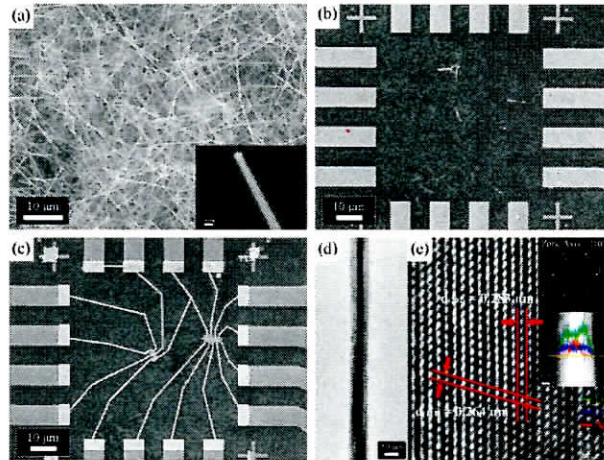

Fig. 1 Top-view FESEM and FETEM images of nanowire structures. (a) As-prepared gold-in-Ga_2O_3 core-shell nanowires on silicon substrate. The inset of part a is a high-magnification FESEM image of a core-shell nanowire with a diameter around 200 nm. The center bright area is the gold core and outer dark region is the Ga_2O_3 shell layer. (b) Chip SEM image. A core-shell nanowire is placed in the chip area with a three axis joystick micromanipulator under optical microscope. (c) As-prepared chip FESEM image. (d) Low-magnification FETEM image with a clear dark area in the center. (e) High resolution image and diffraction pattern. The zone axis is [101] direction and the d-spacings of $(20\overline{2})$ and $(11\overline{1})$ were 0.283 and 0.264 nm, respectively. Composition analysis in the inset of part e shows that the center area is gold core and the outer region is the Ga_2O_3 layer.

2. Fabrication of Gold-in-Ga_2O_3 Nanowire Chips

Gold-in-Ga_2O_3 core-shell nanowires were synthesized on an amorphous SiO_2 substrate with commercial Ga powders (purity 99.9999%) source and size controlled gold nanoparticles catalyst through the vapor-liquid-solid (VLS) growth in the three-zone heating horizontal furnace at a pressure of 1×10^{-2} Torr. Annealing was carried out at 800 °C with a ramping rate of 20 °C/min for 30 min. The morphologies and crystal structures were analyzed by field-emission scanning and transmission electron microscopes. In order to investigate the electron transport behaviors of gold-in-Ga_2O_3 core-shell nanowires, we have fabricated the single nanowire devices on the heavily doped n type silicon wafer covered with 500 nm thick thermally grown SiO_2 layer as the insulating layer. On the top of it, we have employed photolithography to define platinum electrodes. Single nanowire is picked up onto the measurement chip with a three-axis joystick micromanipulator having glass tips via static electricity under optical microscope. The titanium contact metal and gold antioxidant metal electrodes are deposited to connect to the platinum electrodes by e-gun system and defined by electron beam lithography. The electrical characteristics are measured with a Keithley 4200 in atmospheric air at room temperature.

3. Results and Discussion

Figure 1a shows an FESEM image of high-density gold-in-Ga_2O_3 core-shell nanowires. Highly uniform nanowires were synthesized through the vapor-liquid-solid (VLS) mechanism with gold nanoparticles as catalysts on top of nanowires. The inset shows a high-magnification FESEM image of the core-shell nanowire with a diameter around 200 nm. There is a clear gold core in the center. To measure the resistive switching of these nanowires, we transferred the core-shell nanowires from the substrate onto the electrical measurement chip by three-axis joystick micromanipulators as shown in Figure 1b. Using the electron beam lithography and e-gun system, several titanium and gold metal electrodes were defined onto a single nanowire as shown in Figure 1c. Figure 1d shows the

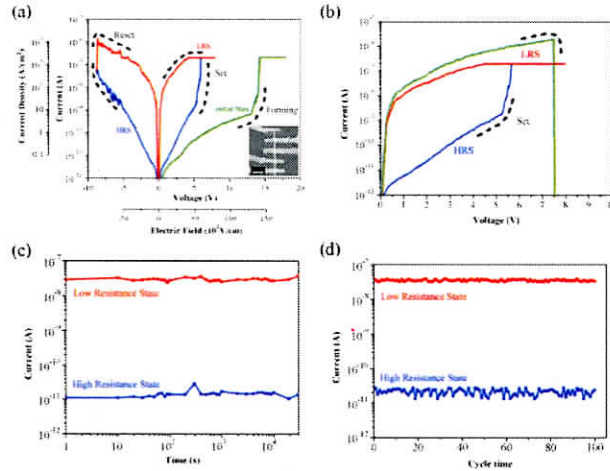

Fig. 2 (a) I−V characteristics of a single gold-in-Ga_2O_3 core-shell nanowire showing a bipolar switching and the inset is the chip FESEM image. The green, blue and red represent the initial state, off state and on state, respectively. (b) I-V characteristic of a single gold-in-Ga_2O_3 core-shell nanowire with voltage sweeping in the same polarity of bias as that in the forming process. The blue, red and green curves demonstrate the HRS, LRS and second time positive voltage sweep, respectively. It burns off and breaks down directly at about 2×10^{-6} A due to large Joule heating. The retention test curve in part c illustrates that on and off states can last more than 30000 s. The endurance test in part d shows that the on/off ratio is more than 3 orders of magnitude and the cycle number is over 100 cycles.

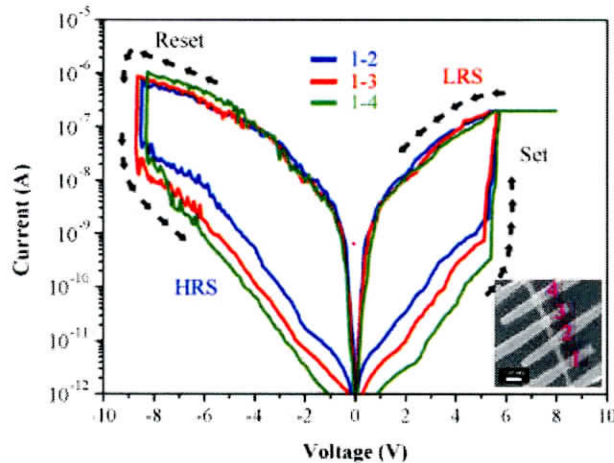

Fig. 3 Bipolar switching characteristic of a single gold-in-Ga_2O_3 core-shell nanowire with different distances between electrodes and the inset is the FESEM chip image. The blue, red and green curves are for electrode distance at 900, 1630, and 2440 nm, respectively. These set and reset voltages are almost the same with different distances.

low-magnification FETEM image with a clear dark area inside the light shell layer. The diameter of this nanowire was about 50 nm. Energy dispersive X-ray analysis suggests that the center area is the gold core and the outer region is the Ga_2O_3 layer as shown in the inset of Figure 1e. Figures 1e shows the high-resolution image and the diffraction pattern of Ga_2O_3 shell layer. The zone axis was [101] direction and the d-spacings of $(20\bar{2})$ and $(11\bar{1})$ were 0.283 and 0.264 nm, respectively. Those two values fitted well with the theoretical values of monoclinic Ga_2O_3.

Figure 2a shows the resistive switching characteristics, plotted in a semilogarithmic scale, of core-shell nanowire with a diameter of about 120 nm. The gold core is 40 nm in

diameter and the Ga_2O_3 shell layer has a shell thickness of about 40 nm. The inset shows a corresponding chip FESEM image. Due to the symmetric structure of titanium/gold-in-Ga_2O_3/titanium, we can apply positive or negative biases to perform the resistive switching characteristics. The polarity of set and reset processes is defined by the polarity of every first voltage sweep. By performing the forming process (green line), the current increased from 2.4×10^{-12} A at 1 V to the current compliance, 2×10^{-7} A at 14.3 V. This sharp increase of current indicates that gold-in-Ga_2O_3 core-shell nanowire may have two stable states. After the forming process, this core-shell nanowire exhibits a bipolar resistive switching behavior, i.e. the set and reset processes are controlled by the polarity of electric field. The set voltage (V_{set}) defined as the voltage needed to drive HRS (blue curve) to LRS (red curve) transition is at around 5 V or 5×10^4 V/cm. Changing from the LRS to HRS state, the reset voltage (V_{reset}) takes place at about -8.5 V or -8.5×10^4 V/cm. The operating electric field is comparable to those of thin film devices[23] and single nanowire devices.[24] The higher driving voltages required in nanowires are caused by the larger electrode distance as compared to that of thin film. In order to verify the type of resistive switching of the gold-in-Ga_2O_3 core-shell nanowire, we have performed the reverse and parallel polarity voltage sweeps after the set process. Parallel polarity means the same voltage polarity as used in the set process. Reverse polarity takes the opposite. Compared to Figure 2a, Figure 2b shows the I−V characteristics of core-shell nanowires with applied positive bias (parallel polarity) after set process. The blue, red, and green curves demonstrate the HRS, LRS, and second-time positive voltage sweep, respectively. The current state of green curve is higher than HRS but the nanowire burns off and breaks down directly at about 2×10^{-6} A due to large Joule heating. It does not show a high resistive state as a typical unipolar switching device. Data from parts a and b of Figure 2 indicate that gold-in-Ga_2O_3 core-shell nanowire exhibits bipolar resistive switching behavior rather than unipolar. As far as conduction mechanism is concerned, this result resonates with other published studies.[25,26] During the set process, oxygen ions (O^{2-}) migrate toward the anode to form oxygen-vacancy conducting filaments inside the Ga_2O_3 layer. After the set process, the oxygen reservoir forms at the anode side because of the accumulation of O^{2-} ions.[25] For reset, it can occur either under the reverse polarity bias (bipolar behavior) to terminate the conducting filaments by migrating O^{2-} ions from the anode to Ga_2O_3 layer because drift and diffusion forces perform at the same direction or under the same polarity bias (unipolar behavior) without the interfacial barrier since the diffusion force can overcome the drift force.[26] Noble metals such as platinum, gold and rubidium used as electrodes on both ends typically show unipolar behavior because noble metal is resistant to oxidation and no interfacial layer forms. However, most electrodes made of oxidizable materials such as titanium and aluminum may show bipolar characteristics due to the formation of an interfacial layer to act as the barrier for O^{2-} ions migration.[26] Our nanowire devices having titanium electrodes show they are bipolar. That is consistent with what reported in literature about bipolar behavior with titanium as the electrode in which an interface layer forms. Parts c and d of Figure 2 show the retention behavior and the switching endurance of gold-in-Ga_2O_3 core-shell nanowire, respectively. The LRS and HRS were demonstrated to remain at least 3×10^4 s at a bias of 2 V and the on/off (LRS to HRS) ratio was over 10^3. The high on/off ratio is desired in commercial memory devices. A smaller but still impressive on/off ratio of 10 can be obtained at an even lower bias of 0.2 V. In addition to the high on/off ratios, the switching endurance of these nanowire devices lasts at least 100 cycles of set and reset processes, and the operation current can reduce to tens of nanoampere for low power consumption.

As reported in numerous published papers, there are many great features in resistive switching memory devices such as faster writing speed, smaller device feature size, lower programming voltage and multistate memory in RRAM. Nevertheless, the V_{set} and V_{reset} are found to depend on the distance between two electrodes. As the distance increases, it needs a larger driving

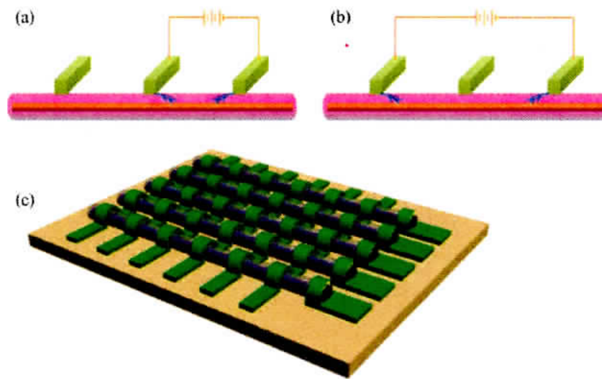

Fig. 4 Schematic drawings depicting conducting paths and the transport mechanism that explain the properties of invariant V_{set} and V_{reset} against different distances between electrodes. (a) Demonstration that the oxygen vacancy filament connects to the gold core in the center of nanowire because the distance between two electrodes, 900 nm, is much larger than the thickness of Ga_2O_3 shell layer, 40 nm. (b) Indication that the oxygen vacancy channel can link to the gold core due to the smaller diameter compared to the distance. (c) Illustration of a possible resistive switching device array picture formed gold-in-Ga_2O_3 core-shell nanowires.

voltage to set and reset the devices.[27-29] This distance-dependent voltage variation makes the precise control of the thickness of insulation layer critical to the fabrication of resistive switching devices. In contrast, gold-in-Ga_2O_3 core-shell nanowire can provide the distance independent V_{set} and V_{reset}. Figure 3 shows the resistive switching characteristics with different distance between electrodes, and the inset indicates an FESEM image of a device with six metal electrodes. This core-shell nanowire is composed of a gold core of 50 nm in diameter and Ga_2O_3 shell layer of 40 nm in thickness. The blue, red and green curves represent the resistive switch characteristics corresponding to different electrode distances at 900, 1630, and 2440 nm, respectively. These three curves demonstrate that the bipolar switch characteristic and the driving voltages are similar with Vset and Vreset around 5.4 V and -8.5 V, respectively. The almost invariable Vset and Vreset is a unique feature compared with other reports.[27-29] We attribute the invariance to the presence of a highly conductive gold metal core. As the gold core can serve as a conductor channel in the center of core- shell nanowire, the conducting path between two electrodes is dominated by the conductivity path in the Ga_2O_3 layer between the metal electrode and gold core. Therefore, the values of V_{set} and V_{reset} depend mainly on the thickness of the Ga_2O_3 shell layer but not on the length of nanowires. This unique property, i.e. invariant biases of V_{set} and V_{reset}, can greatly enhance the density of cells in a single nanowire device and takes the commercial nanowire memory industry a big step forward.

Parts a and b of Figure 4 illustrate the possible transport mechanism attributed to the observed invariance V_{set} and V_{reset} for different distances between electrodes. As we apply the forward bias between two electrodes, oxygen vacancy filament forms in the Ga_2O_3 shell layer along the direction of electric field. Since the distance between two electrodes, 900 nm, is much larger than the thickness of Ga_2O_3 shell layer, 40 nm, the oxygen vacancy filament tree can form, touch and connect easily to the gold core in the center of nanowire as shown in Figure 4a. As the oxygen vacancy channels form, electrons can transport through the gold core. When we increase the distance to 1630 or 2440 nm in our experiments, the oxygen vacancy filament trees can still link to the gold core due to the smaller Ga_2O_3 shell thickness as compared to the distance between electrodes as shown in Figure 4b. We attribute the finite Ga_2O_3 layer thickness and the conducting gold core to the invariable set and reset voltage in the gold core-Ga_2O_3 shell nanowire structures. Taking advantage of this unique property of invariant biases of V_{set} and V_{reset}, we can realize numerous resistive switching cells in

a single core-shell nanowire by depositing repetitive metal electrodes. A possible design of resistive switching device array is proposed in Figure 4c. The electrodes parallel and vertical to the gold-in-Ga_2O_3 core-shell nanowires would serve as word lines and bit lines, respectively, to write, read and erase data. Because of the invariable V_{set} and V_{reset}, we can apply the same operation voltage between a word line and any one of the bit lines to store information into the resistive switching cells which form below the bit lines. By narrowing the spacing between bit lines, we can achieve high density resistive switching cells in a single gold-in-Ga_2O_3 core-shell nanowire.

4. Conclusion

In conclusion, we have successfully demonstrated invariable set and reset voltages in gold-in-Ga_2O_3 core-shell nanowires, which are synthesized through the VLS growth mechanism. This invariant result because electrons transport through the conducting paths formed at the Ga_2O_3 shell layer and Au metal core. The invariant set and reset voltages against the distance between electrodes makes the fabrication of high-density RRAM devices possible by depositing repetitive electrodes along the nanowires. These gold-in-Ga_2O_3 core-shell nanowires exhibit comparable driving electric field (5×10^4 V/cm for set process and -8.5×10^4 V/cm for reset process) compared to other thin film and single nanowire devices. The on/off ratio more than 3 orders of magnitude at 2 V is large enough to make effective resistive switching devices. A smaller but still impressive on/off ratio of 10 can be obtained at an even lower bias of 0.2 V. In addition, the retention time and the endurance cycles are more than 3×10^4 s and 100 cycles, respectively.

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Optical and Surface Recombination Properties of Compound Surface Textures for Heterojunction Solar Cells

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Abstract

The uniform compound structures were performed using metal-assisted chemical etching technique. Combined with defect removal etching (DRE), the reflectance is still significantly suppressed, but the carrier lifetime can be strongly improved by controlling the morphology of nanostructures, benefiting for Si heterojunction solar cells.

1. Introduction

Surface passivation is an important issue in a-Si:H/c-Si based heterojunction solar cells. To obtain desirable surface passivation, the surface area should be as small as possible (e.g., flat surface). However, because of the high reflective index of Si, the flat surface of Si causes up to 40 % of the incident light reflected, which severely limits device performances. Fabricating nanostructure is an effective way to reduce the reflection of light for solar cells but also aggravates the surface recombination by increasing the surface area. Therefore, a crucial challenge in heterojunction solar cell is to break the balance between surface recombination and light absorption losses.

In this work, the uniform compound structures were performed using metal-assisted chemical etching technique. Combined with defect removal etching (DRE), the reflectance was measured and the defect or contamination on the surfaces was monitored through the minority carries lifetime measurements and XPS measurement. The results shows that the reflectance is significantly suppressed, and the carrier lifetime would slightly reduce by controlling the morphology of nanostructures.

2. Description of approach and techniques

First, the Si micropyramids were fabricated on n-type CZ monocrystalline Si(001) substrates via an anisotropic etching process using a solution of potassium hydroxide (KOH) and isopropyl alcohol (IPA) at 85 °C. After 20 min treatment, micropyramids were formed with width of 10 to 15 μm. Subsequently, a 30-nm-thick Ag layer was deposited on the micropyramids using the electron beam evaporation. The large-area and uniform compound structures were obtained by immersing the Ag-covered substrates in the etching solution of HF/H2O2/H2O for 30 s at room temperature. The isotropic DRE process was investigated to control the final surface morphologies and remove the surface defects.

The total reflectance over the wavelength regions from 300 to 1130 nm was measured by a JASCO V-670 UV-VIS-IR spectrometer. The quasi-steady-state photo-conductance technique was used to measure the effective carrier lifetimes of the samples.

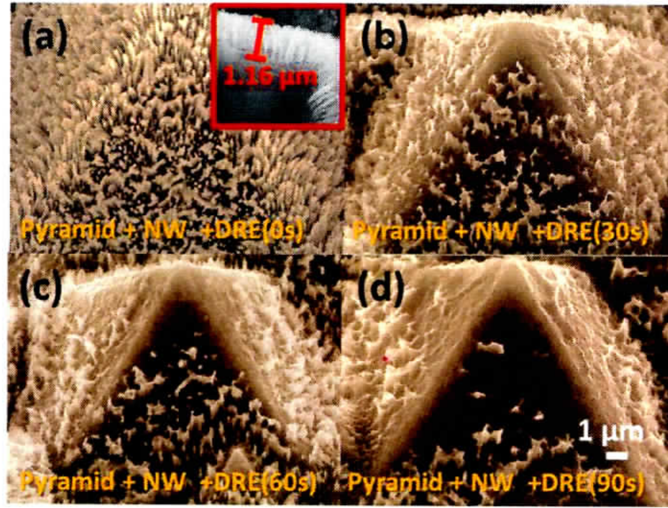


Fig. 1 (a) The SEM images of hierarchical structures with different DRE durations at 0, 30, 60, and 90 s, respectively.

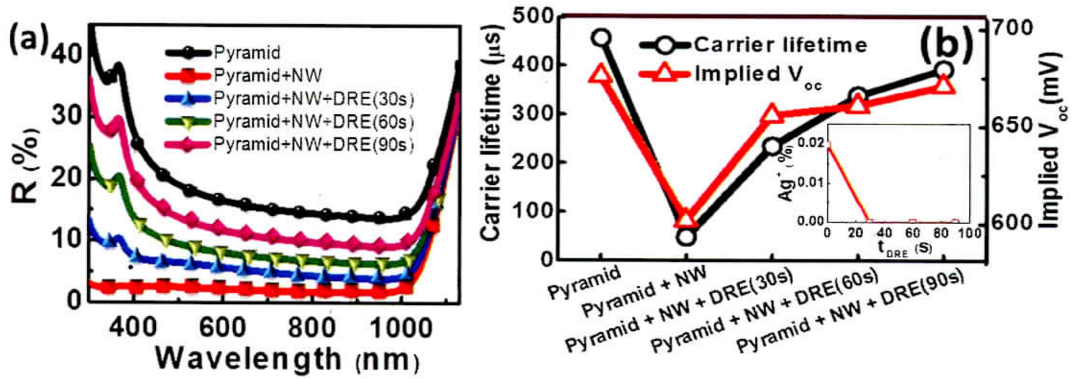
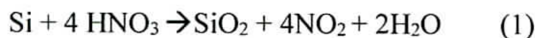


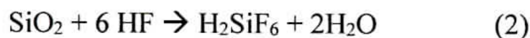
Fig. 2 (a) Total reflectance over the wavelength regions of 300-1130 nm and (b) the effective carrier lifetime of compound structures with different DRE durations at 0, 30, 60, and 90 s, respectively.

Results and Discussion

The isotropic DRE process was investigated to control the final surface morphologies and remove the surface defects. The DRE solution is mixture of nitric acid (HNO3) and hydrofluoric acid (HF). The reactions were described as the following equation:[1]



$$Si + 4\,HNO_3 \rightarrow SiO_2 + 4NO_2 + 2H_2O \qquad (1)$$



$$SiO_2 + 6\,HF \rightarrow H_2SiF_6 + 2H_2O \qquad (2)$$

According to the mass-transfer theory, etch rates at peaks are higher than etch rates at valleys because of varying mass-transfer film thickness;[2, 3] hence the NWs become shorter, and the density is lower, benefiting the PECVD deposition. The contaminated surface by Ag^+ and Ag particles can also be etched away. Moreover, the HNO_3 oxidation of Si method forms atomically smooth SiO_2/Si interfaces, so that the atomically smooth Si surfaces are formed after etch-off of the SiO_2 layer.[4] In this way, we reduced the density of NWs, removed the Ag contamination, and made the NWs' surface atomically smooth.

The morphology changes after DRE process were observed by scanning electron microscopy (SEM) (recorded at the tilted angle of 45°). Fig. 1 (a)-1 (d) show the

images of compound structures with different DRE durations at 0, 30, 60, and 90 s, respectively.

In order to evaluate the AR property of compound structures with DRE, the R_{total} of compound structures with different DRE durations was measured, as shown in Fig. 2 (a). The average R_{total} of the hierarchical structures without DRE is reduced from 19.70 to 3.83 % in the wavelength range of 300-1130 nm. In addition to the reflectance measurement, the effective carrier lifetime measurement is the way to evaluate the implied V_{oc}, verifying the damage removal effect. Fig. 2 (b) is the effective carrier lifetimes of all samples after iodine passivation. The τ_{meas} greatly drops after metal-assisted chemical etching, indicating high surface defects and carrier trapping centers occurred on the compound structures surface. Then, the τ_{meas} significantly increases after 30 s DRE, demonstrating the effective reduction of defect and contamination of the surface. To further analyze the influence of Ag contamination, Ag^+ content was detected by XPS as shown in the inset of Fig. 2 (b). The Ag^+ content decreases with t_{DRE} from 0.02 % (t_{DRE} = 0 s) to 0 % (t_{DRE} = 30 s), exhibiting the Ag contamination is completely removed after 30 s DRE. The reduction of Ag contamination is not only because that the Ag^+ contamination was etched away with the etched surface, but also the Ag remaining at the bottom can be removed by HNO3. The solutions become more easily to penetrate into the NWs due to the decreases of NWs' density and length. Then, the τ_{meas} further increases with DRE duration. Since the Ag^+ contamination is already effectively removed after 30 s DRE, the increase in τ_{meas} can be attributed to the atomic surface roughness removal and the atomically smooth Si surfaces creation.

To balance the R_{total} and τ_{meas}, we can obtain the optimized condition for Si heterojunction solar cells.

3. Conclusion

Using metal-assisted chemical etching combined with DRE, the increased surface area does not greatly lower the implied V_{oc} compared to the micropyramid structures, making the high efficiency nanostructured HIT solar cells possible to achieve.

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Fabrication and Electrical Property of Au@SnO2 Nanowires

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Abstract

Via Vapor-Liquid-Solid (VLS) mechanism, Au@SnO2 core-shell nanowires were fabricated on SiO2 substrates with using of high purity Sn metal on which Au nanoparticles were dispersed. According to HRTEM observation, Au@SnO2 core-shell nanowires were single crystal and growing along [001] direction. The resistivity was identified as 7.93×10-3 Ω-cm by I-V measurement.

1. Introduction

Highly sensitive and versatile chemical sensors have attracted considerable attention in recent years due to many types of harmful particles in our daily environment. In the modern city, economic development usually accompanies environment pollution. The lower detection limit, rapider reaction time and capability to sense many types of pollutant are significant to chemical sensors. Unfortunately, most of existing sensors based on metal oxide thin film structure have limited working temperature and concentration; they usually should work at elevated temperature and with higher detection limit which is not enough to apply in life (1). In last few decades, nanotechnology has been paid a lot of attention due to their novel properties and potential applications different from their bulk materials (2). Nanostructures such as nanowires, nanotubes and nanobelts with ultrahigh surface-to-volume ratios can provide larger reactive area and further improve the detection limitation (3-5). As mentioned above, nanowire is one of the most potential materials to fabricate chemical sensors. In this study, we can successfully synthesized Au@SnO_2 core-shell nanowires that composed of continuous single crystal Au nanowire core and single crystal SnO_2 shell layer through VLS growth mechanism. SnO_2 is an n-type semiconductor material with a direct band gap 3.6eV, which also has some particular optoelectronic properties (6). This unique Au@SnO_2 core-shell nanowire has great potential to be a gas sensor because of Au core in the middle of nanowire which makes the electrical properties measurement distinctly.

2. Experimental

Au@SnO2 core-shell nanowires were fabricated by simple one-step annealing process. By using high purity Sn metal powders (purity 99.99%) as metal sources and dispersed 150 nm Au nanoparticles on a silica substrate as catalysts. We put these materials into the three-zone heating horizontal furnace. The temperature of the furnace was controlled at 850 ℃ in the sources region, 750 ℃ in the substrates region and the pressure was controlled at 1× 10-2 torr. By controlling the different temperature-holding time and cooling time to synthesize the Au@SnO2 core-shell nanowires. The morphologies, growth orientations and crystal structures were analyzed by field-emission scanning electron microscopes (FESEM, JSM-6500F) and field-emission transmission electron microscopes (FETEM, JEM-3000F). We use electron beam lithography to evaporate electrode on the chip, then measure electrical property of the nanowire.

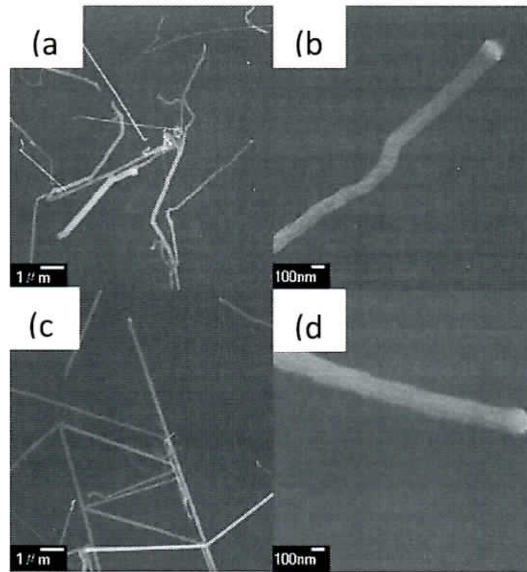

Fig. 1 (a) (b) Temperature-holding time with 30 minutes and cooling time with 30 minutes. (c) (d) Temperature-holding time with 25 minutes and cooling time with 35 minutes

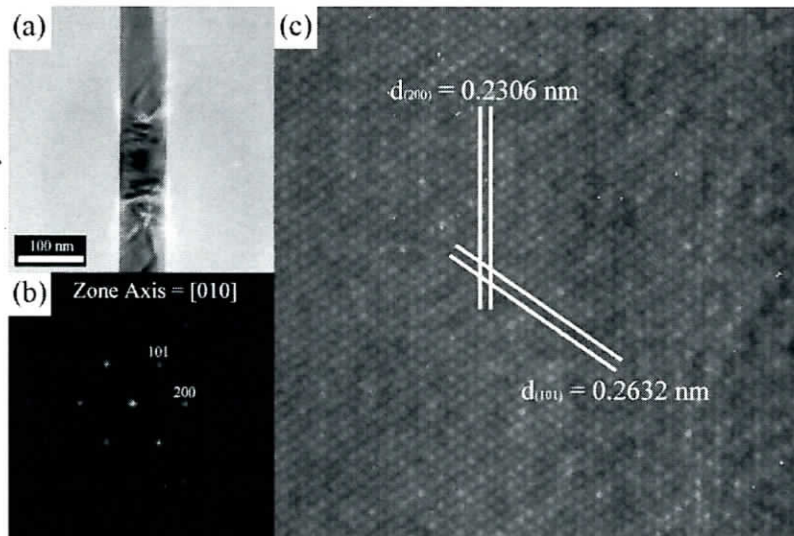

Fig. 2 FETEM images of single Au@SnO2 nanowire. (a) Low-magnification TEM image (b) The corresponding diffraction pattern (DP) and the zone axis was [010]. (c) High resolution TEM image. It shows the spacing of (200) plane was 0.2306 nm and the spacing of (101) plane was 0.2632 nm, respectively.

3. Results and Discussion

Figure 1. shows the FESEM image of Au@SnO2 core-shell nanowires. Figure 1 (a) (b) show the FESEM images of Au@SnO2 nanowires with temperature-holding time with 30 minutes and cooling time with 30 minutes. Figure 1 (c) (d) show the FESEM images of Au@SnO2 core-shell nanowires with temperature-holding time with 25 minutes and cooling time with 35 minutes. We can find Au@SnO2 nanowires can be find in those two conditions steadily.

The FETEM image of a single Au@SnO2 core-shell nanowire was showed in Figure 2. Figure 2 (a) is the low-magnification FETEM image of single nanowire and figure 2 (b) is the

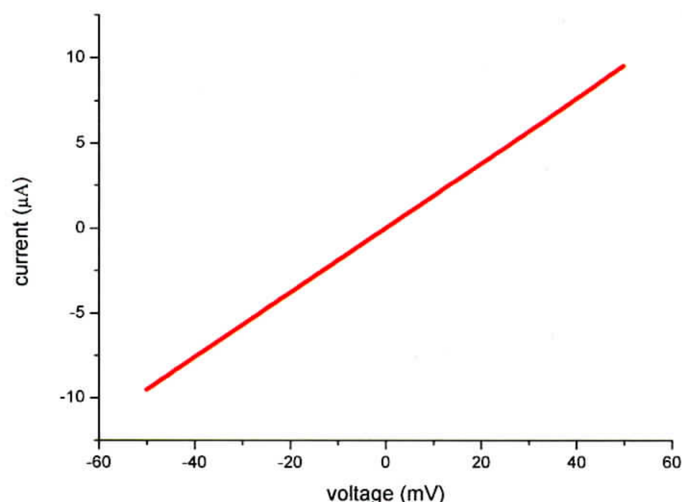

Fig. 3 I-V curve of single Au@SnO2 core-shell nanowire and the resistance was 5277Ω and the resistivity was 7.93×10^{-3} Ω-cm.

corresponding diffraction pattern (DP). It indicated that the zone axis of Au@SnO2 nanowire was [010] direction. Figure 2 (c) illustrates the high resolution TEM image with zone axis in [010] direction. From the FETEM results, the growth direction is along [001] direction. The d-spacing of (200) plane is 0.2306 nm and the d-spacing of (101) plane is 0.2632 nm. It was consistent with reference SnO2 structure face spacing distance.

Figure 3 shows electrical property of single Au@SnO2 core-shell nanowire. By calculating the slope of I-V curve, we can get the resistance about 5277 Ω. In addition, we calculated the resistivity and got the value of 7.93×10^{-3} Ω-cm. Compared to the SnO2 nanowire which reported resistivity was 1.92×10^{-3}Ω-cm, our result was fit to their publications (7).

4. Conclusion

In summary, Au@SnO2 core-shell nanowires were synthesized on silica substrates by using Au nanoparticles as catalyst through VLS mechanism and the temperature-holding time is 25~30 minutes, cooling time is 30~35 minutes. In order to make Au separate out from Sn to form the core of nanowire, we should have the cooling time to change the solubility between the Au and Sn. By using SEM, we can see the morphology of Au@SnO2 core-shell nanowires. In HRTEM image, we can analyze that Au@SnO2 core-shell nanowire were grown along [001] direction. I-V measurement showed that the resistivity of single Au@SnO2 core-shell nanowire was 7.93×10-3 Ω-cm.

Acknowledgement

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